

Fig. 1

1 1 IMAGE SENSOR

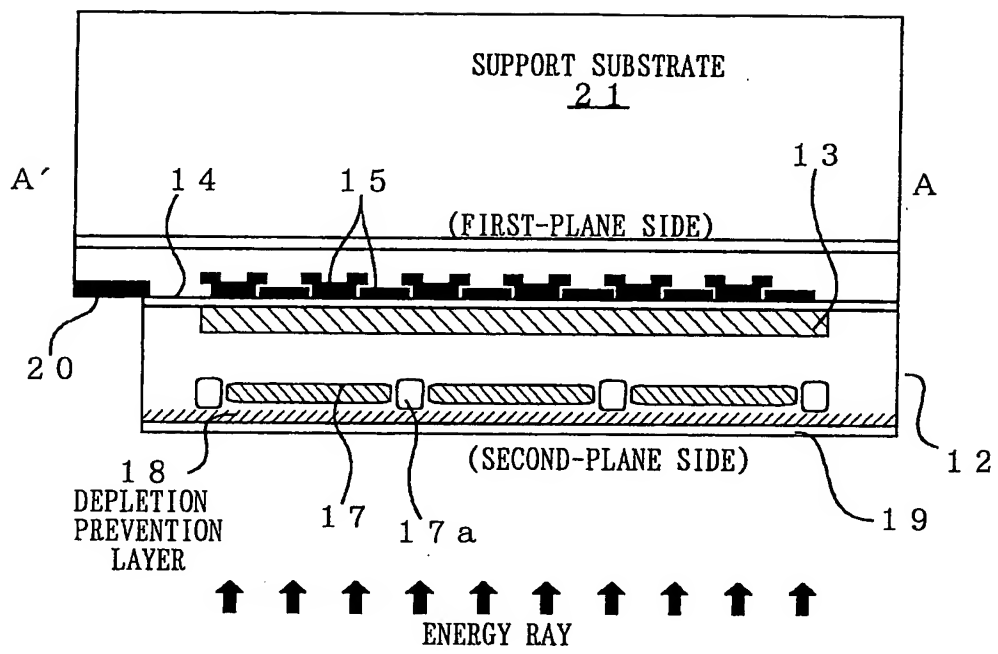


Fig. 2

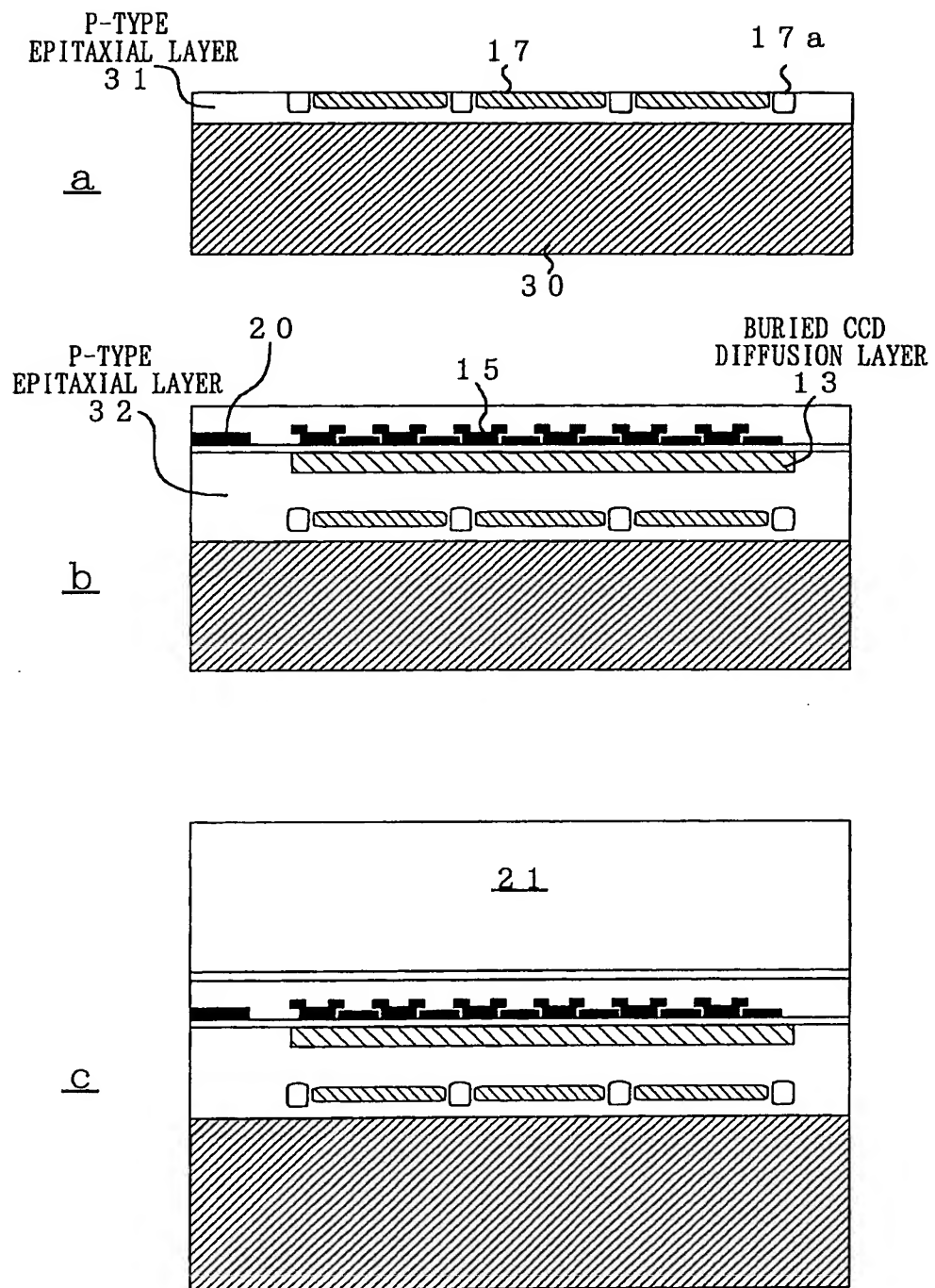
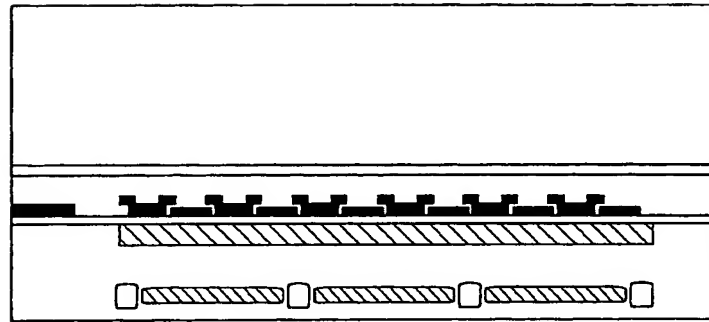


Fig. 3

d



18

DEPLETION PREVENTION LAYER

e

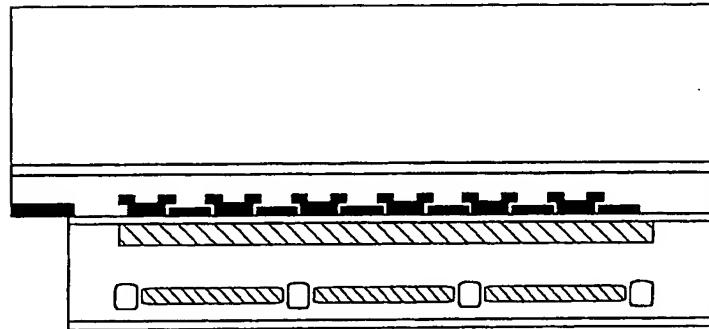


Fig. 4

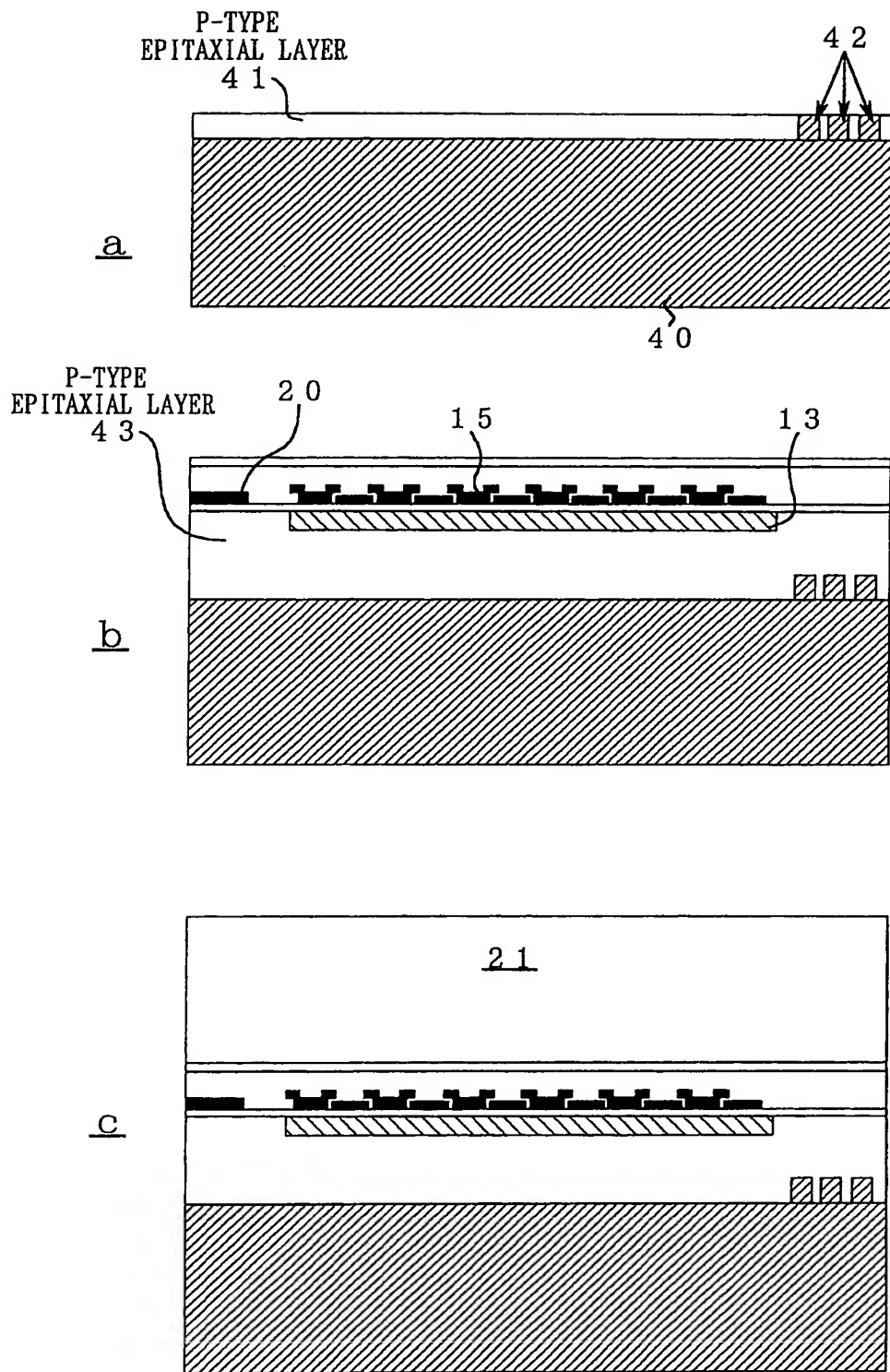


Fig. 5

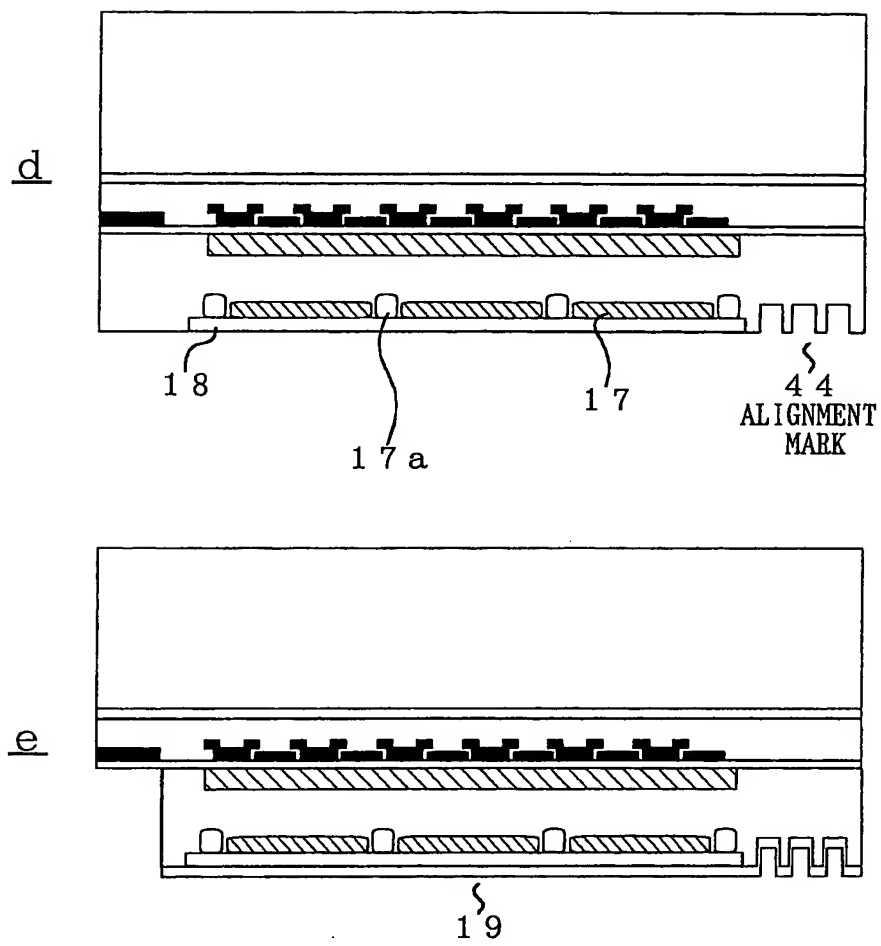


Fig. 6

CHARGE ACCUMULATING OPERATION
AND CHARGE TRANSPORTING OPERATION

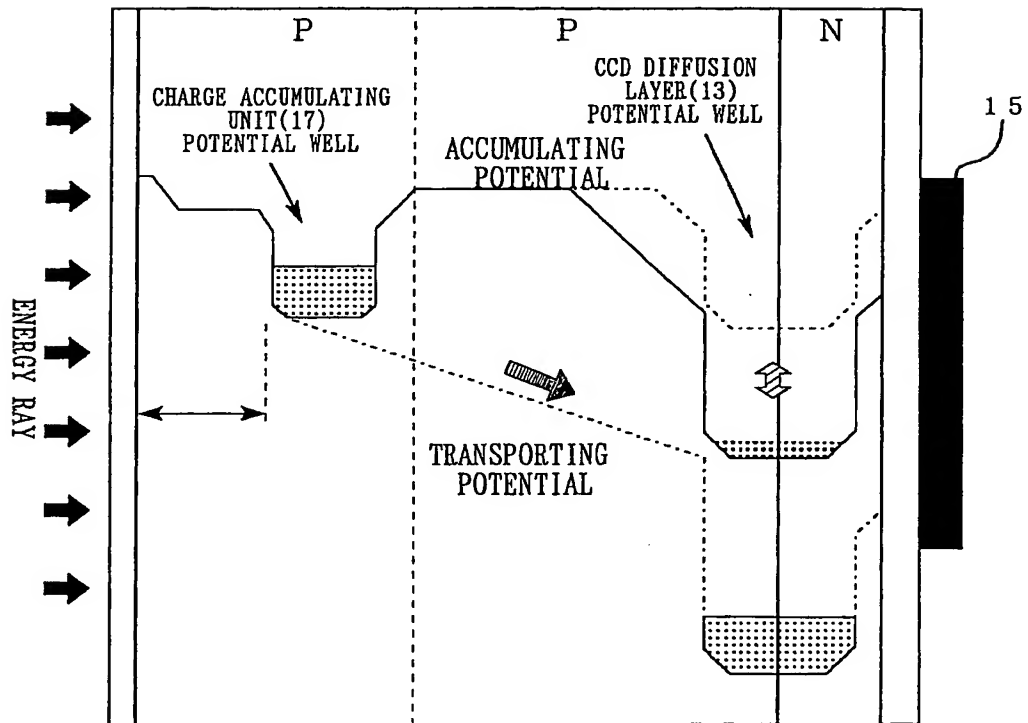


Fig. 7

DARK CURRENT SUPPRESSING
OPERATION ON FIRST-PLANE SIDE

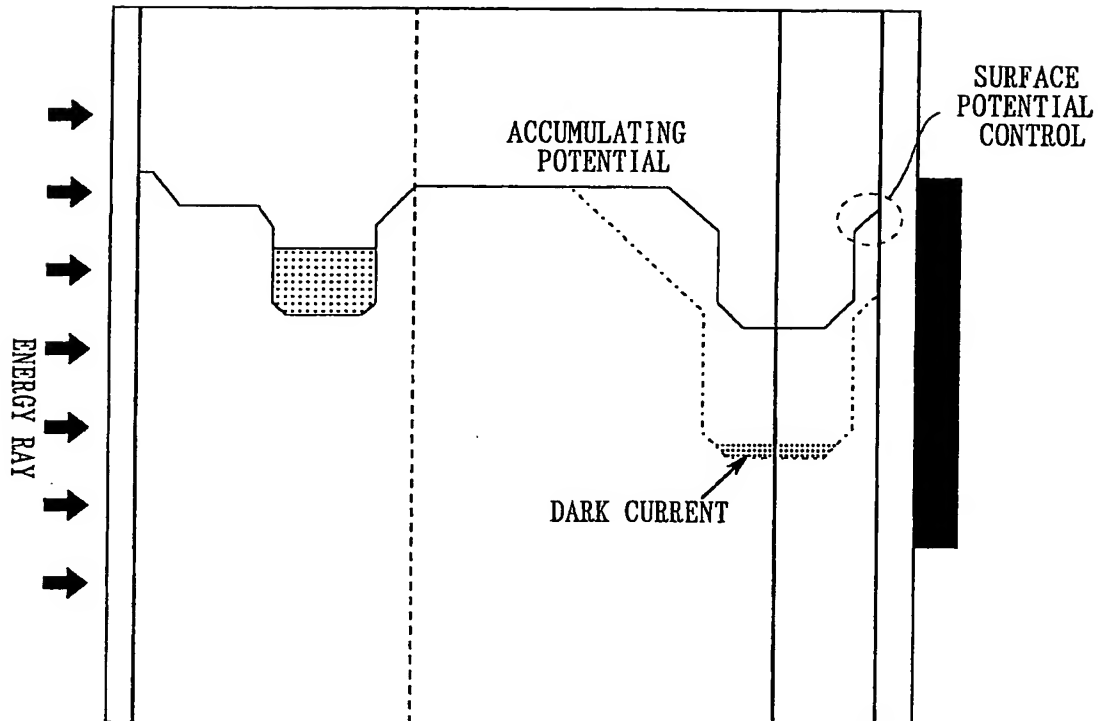


Fig. 8

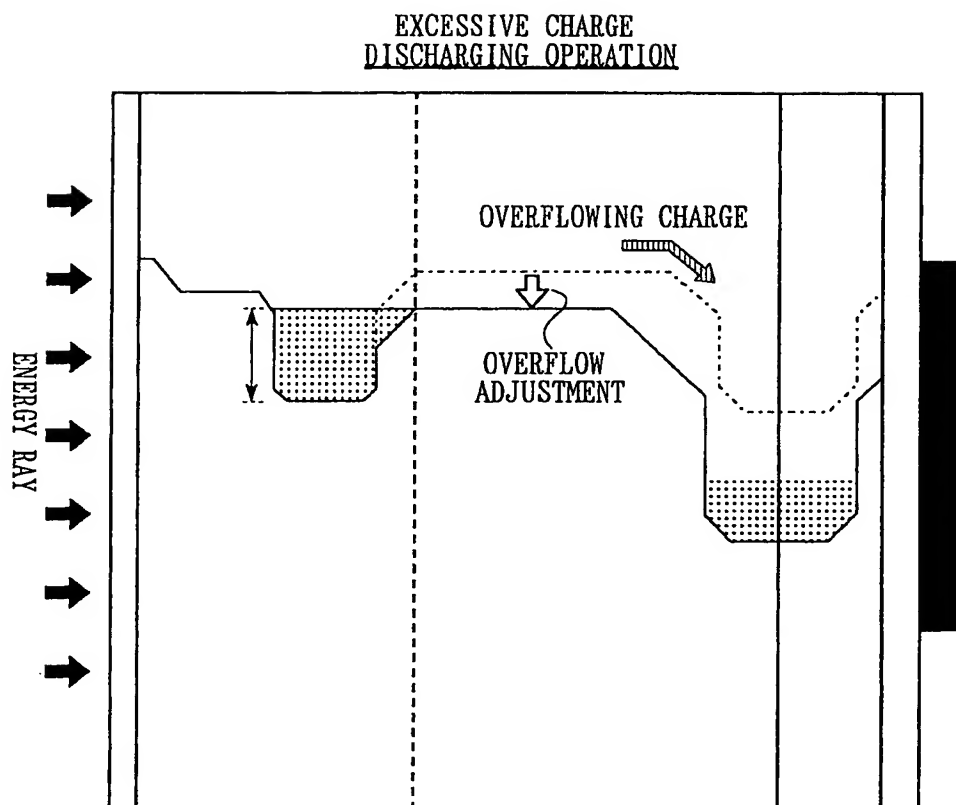


Fig. 9

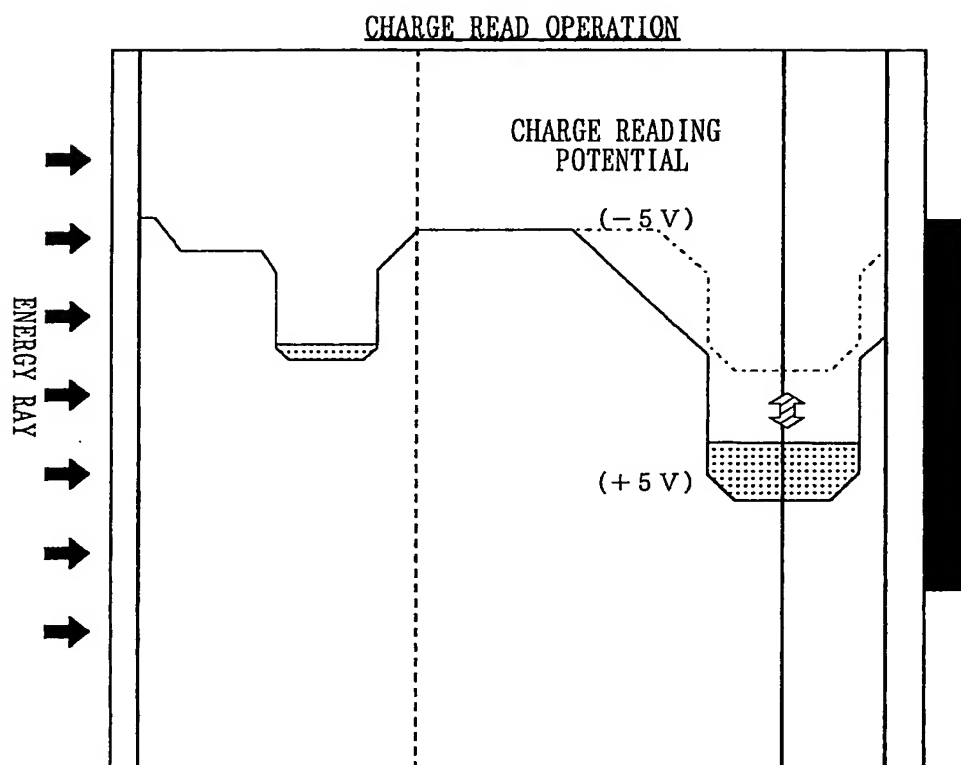


Fig. 10

IMAGE SENSOR
(WELL STRUCTURE TYPE)
51

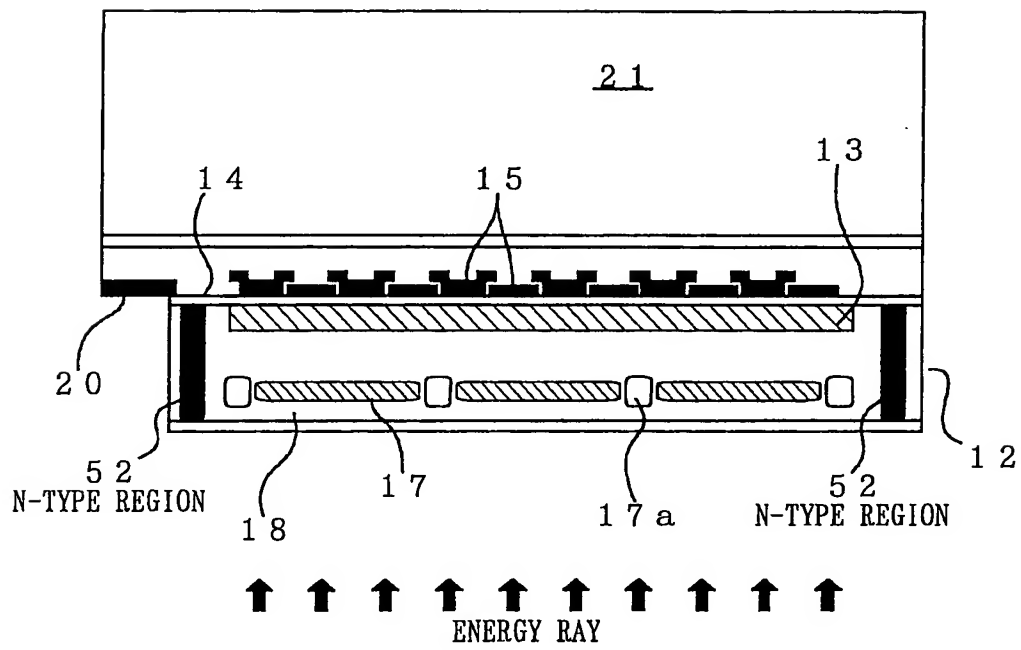


Fig. 11

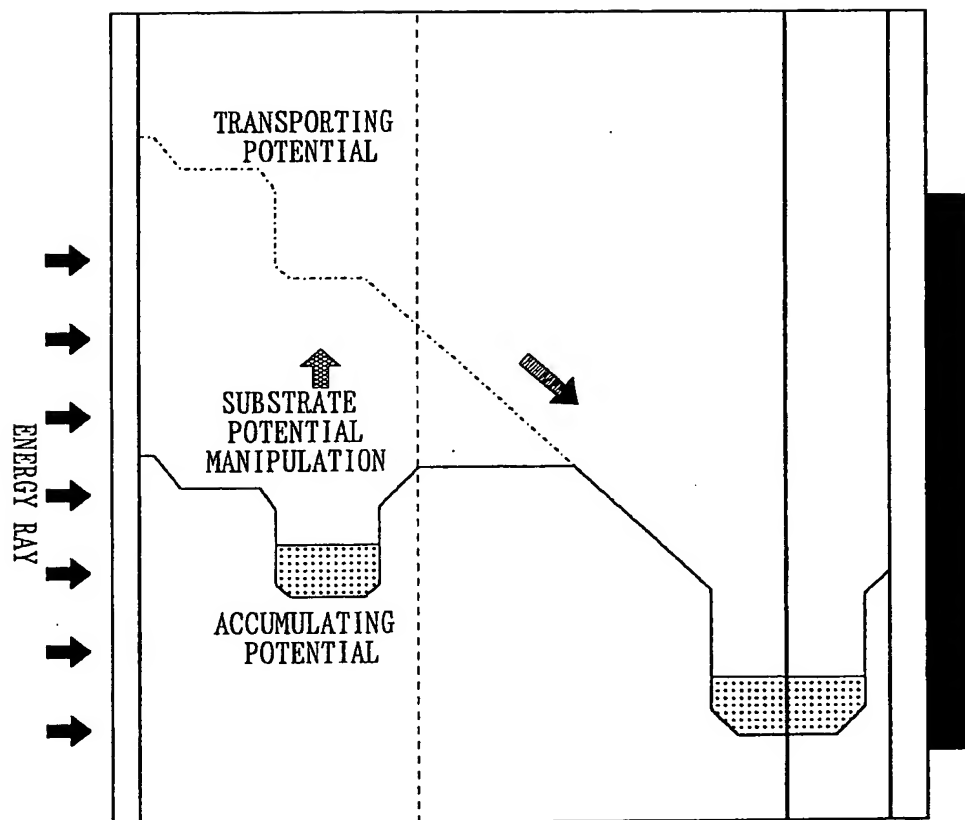


Fig. 12

This diagram shows the top plan view of a semiconductor device. It features a central array of memory cells organized in rows and columns. The array is bounded by a dashed line labeled 17. To the left of the array is a vertical strip of circuitry labeled 15. Above the array is a horizontal strip labeled 13, which includes a buffer symbol and a label B'. Below the array is another horizontal strip labeled 20, with a label B at its center. To the right of the array is a vertical strip labeled 16, which contains four output nodes labeled $\phi V1$, $\phi V2$, $\phi V3$, and $\phi V4$. A label 519 points to a specific row within the array, and a label 24 points to a specific column. The entire device is enclosed in a rectangular frame with small squares at the corners.

Fig. 13

511 IMAGE SENSOR

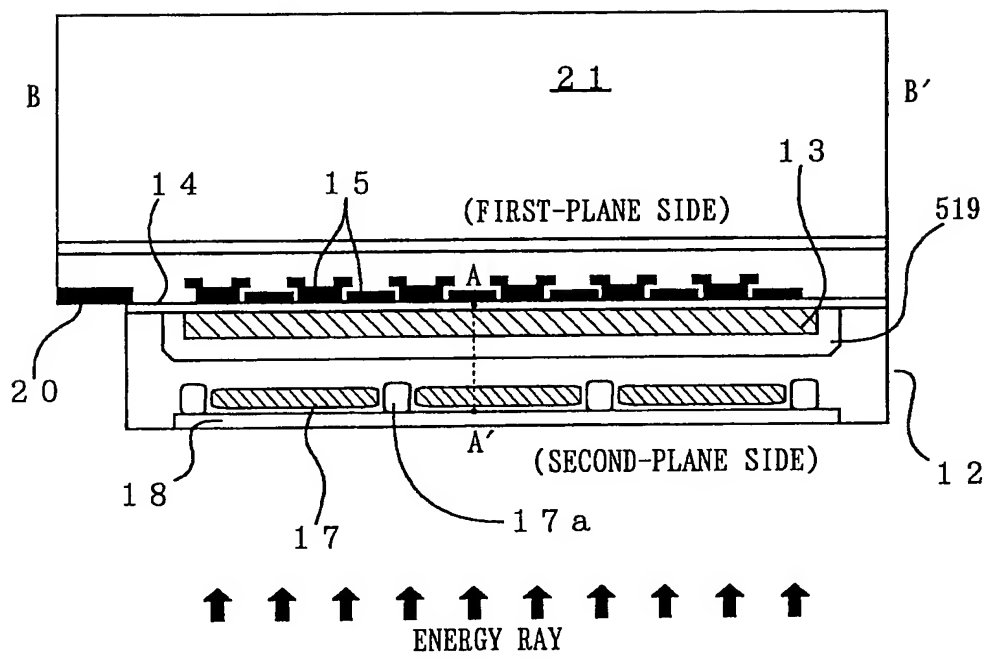


Fig. 14

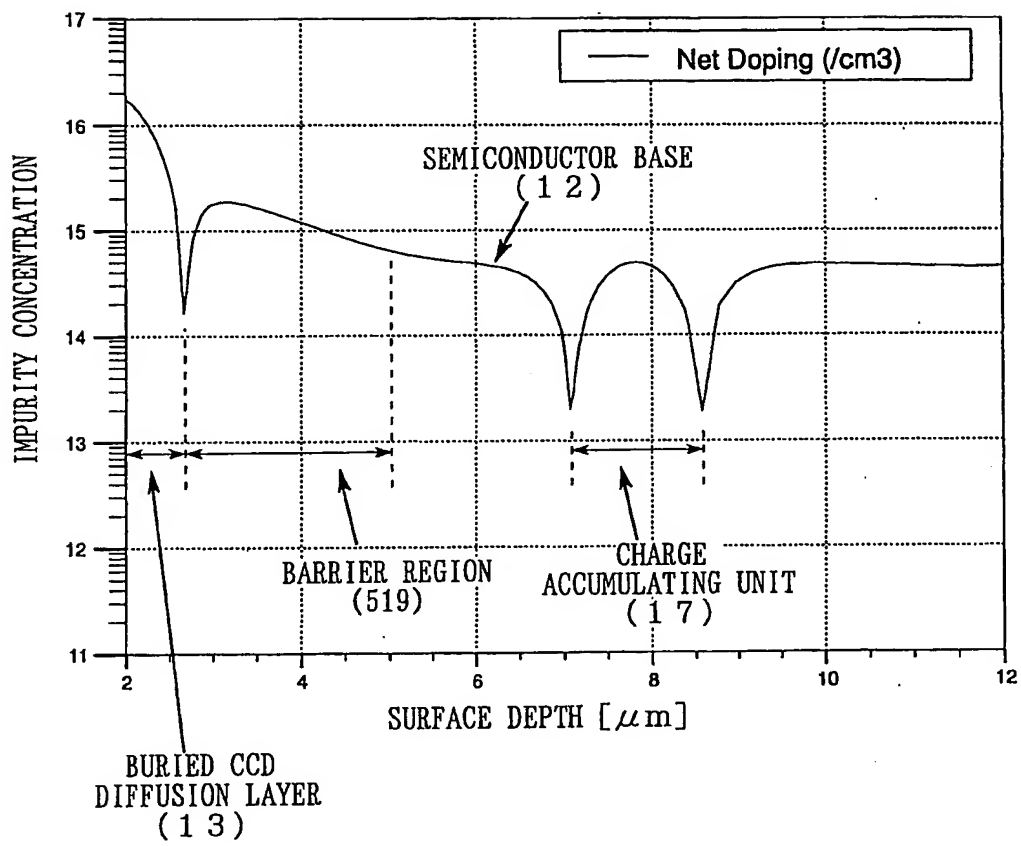


Fig. 15

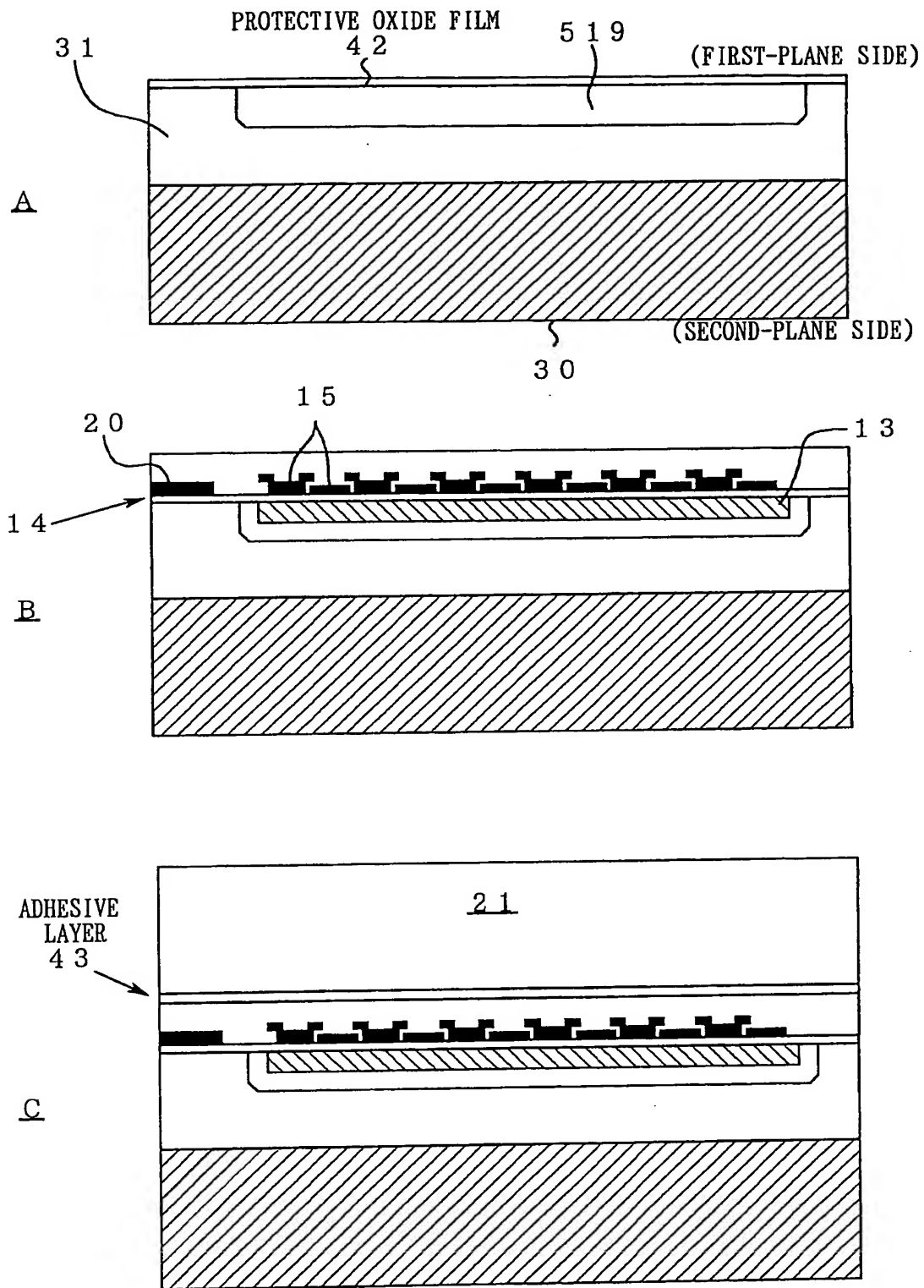


Fig. 16

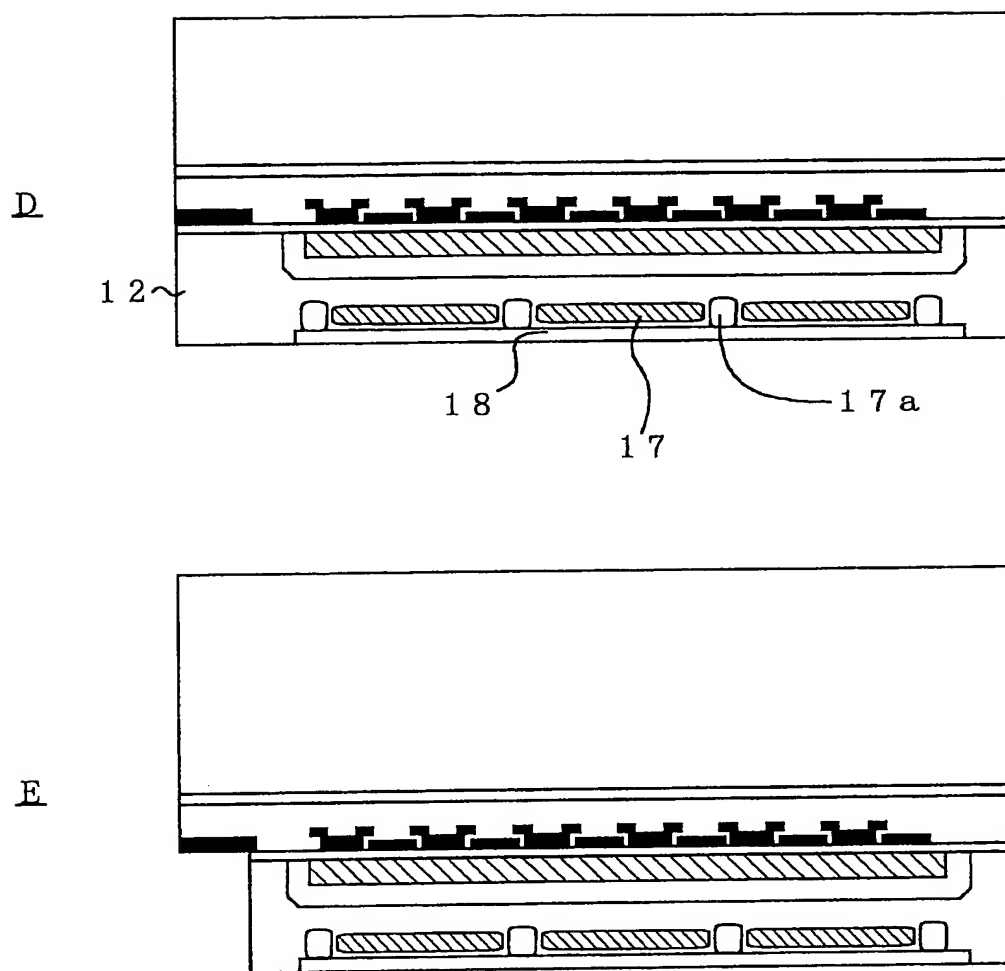


Fig. 17

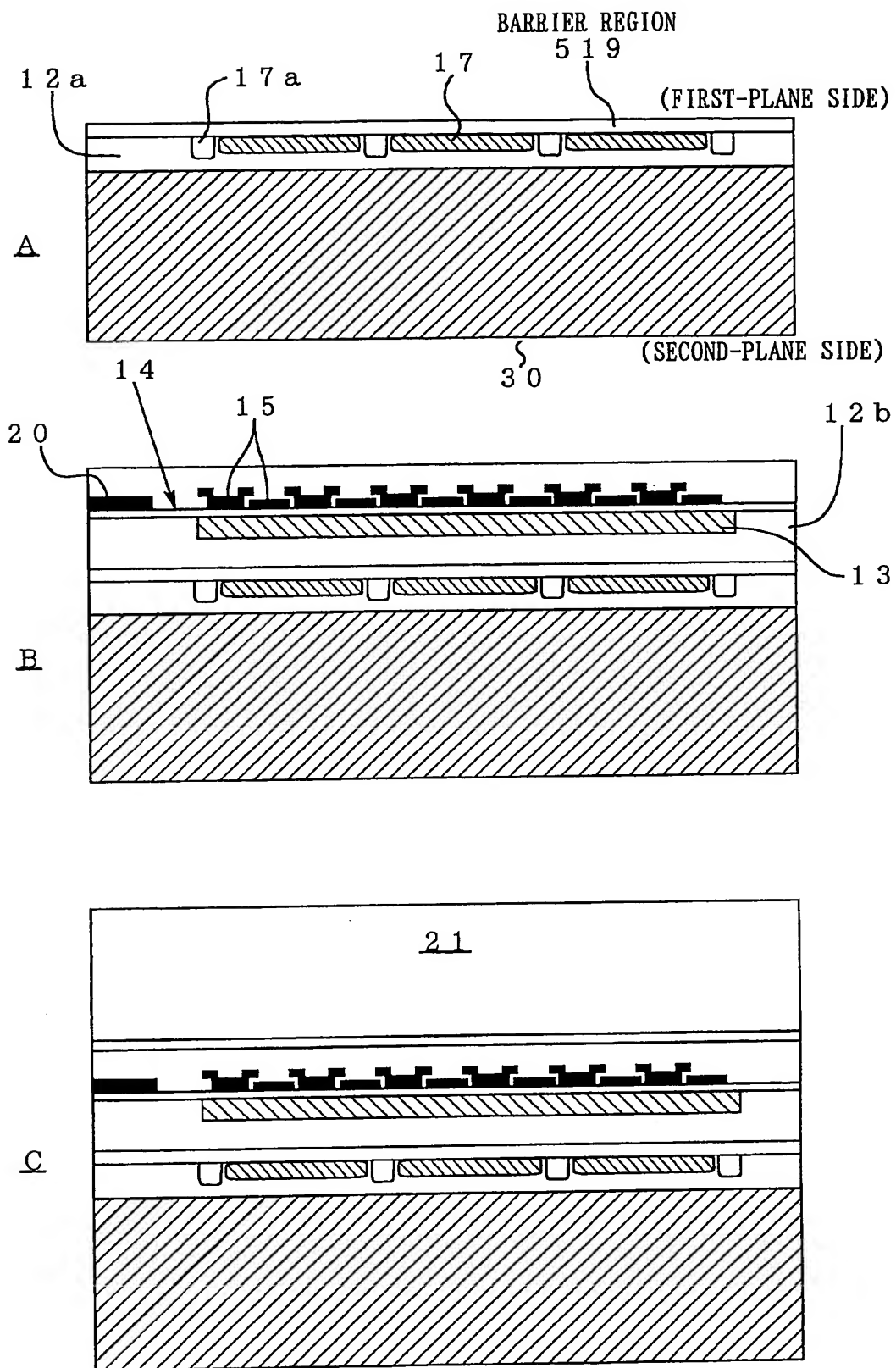
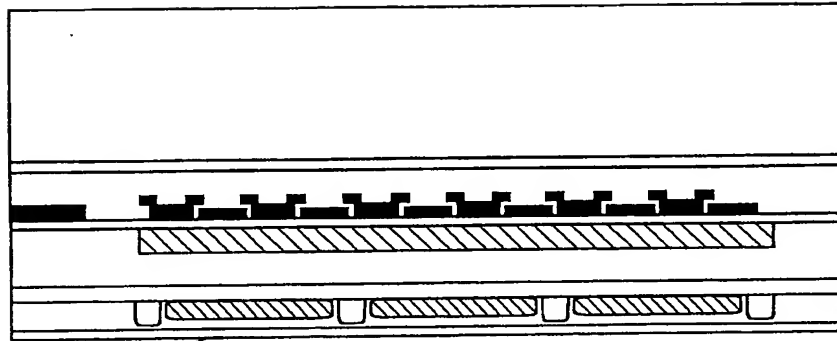


Fig. 18

D



18

E

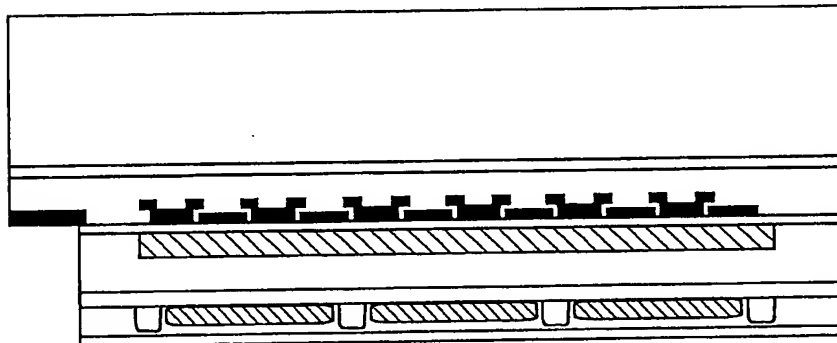


Fig. 19

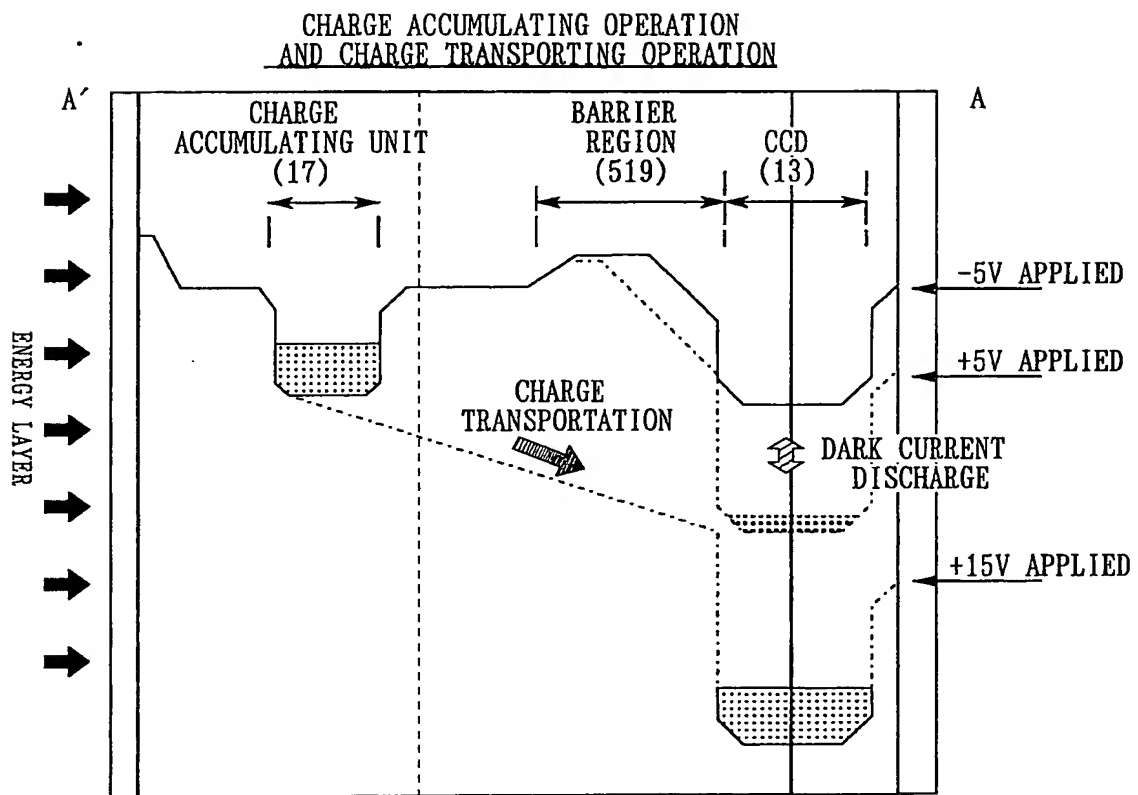


Fig. 20

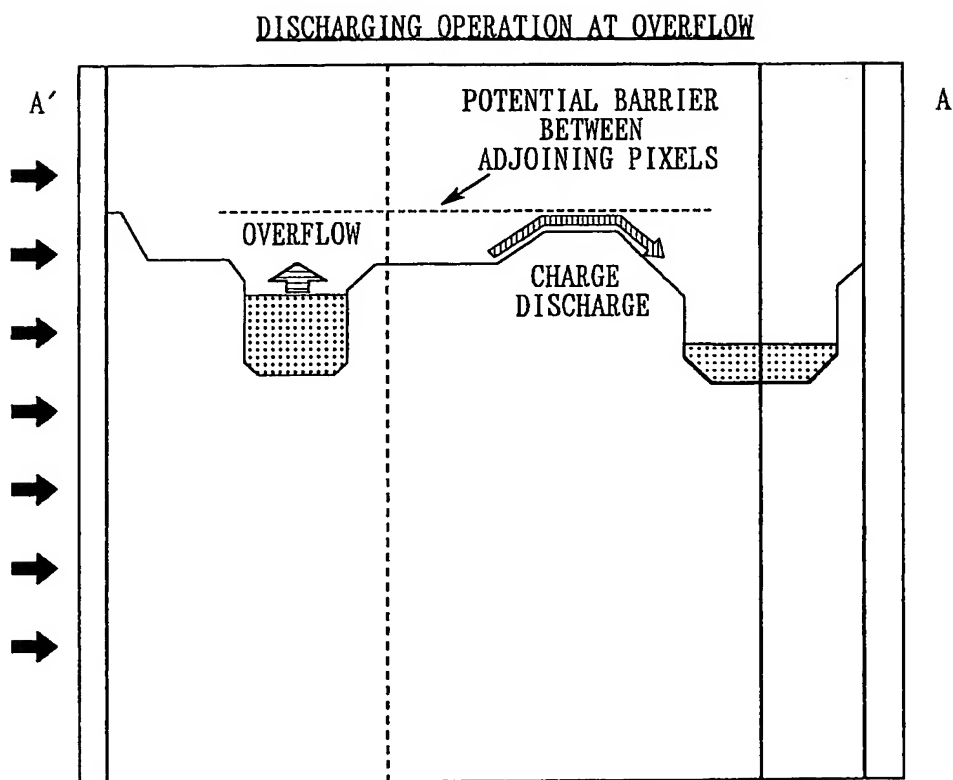


Fig. 21

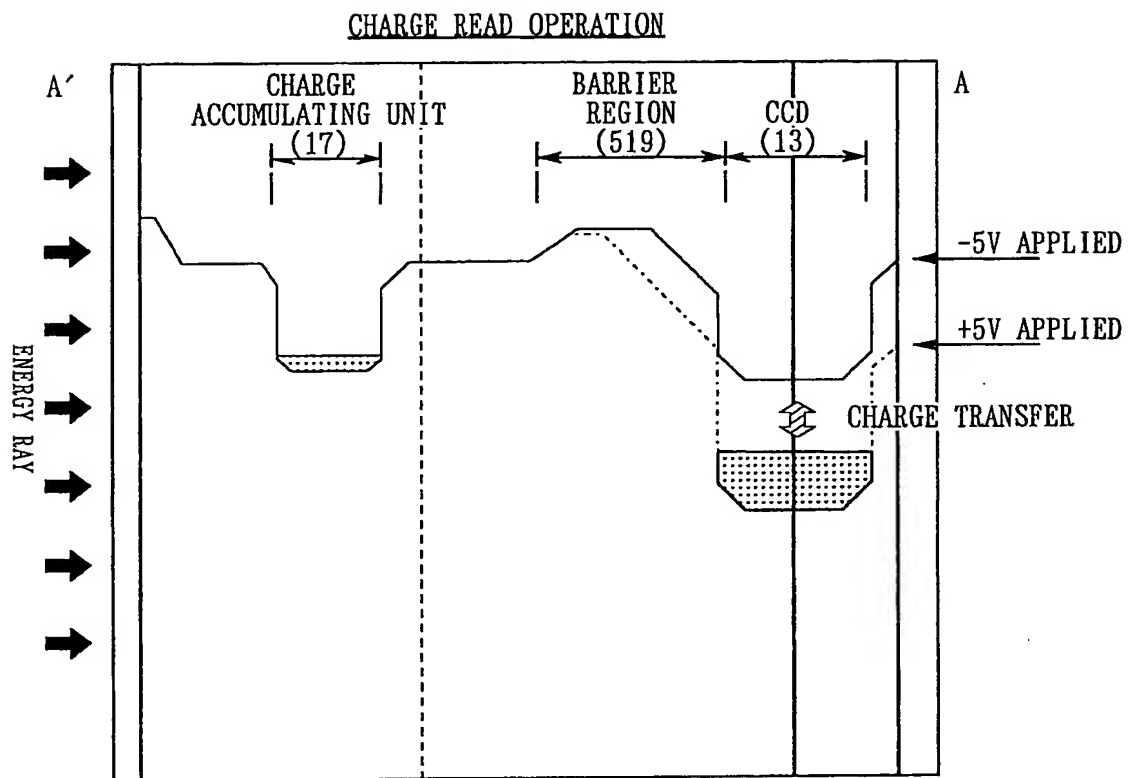


Fig. 22

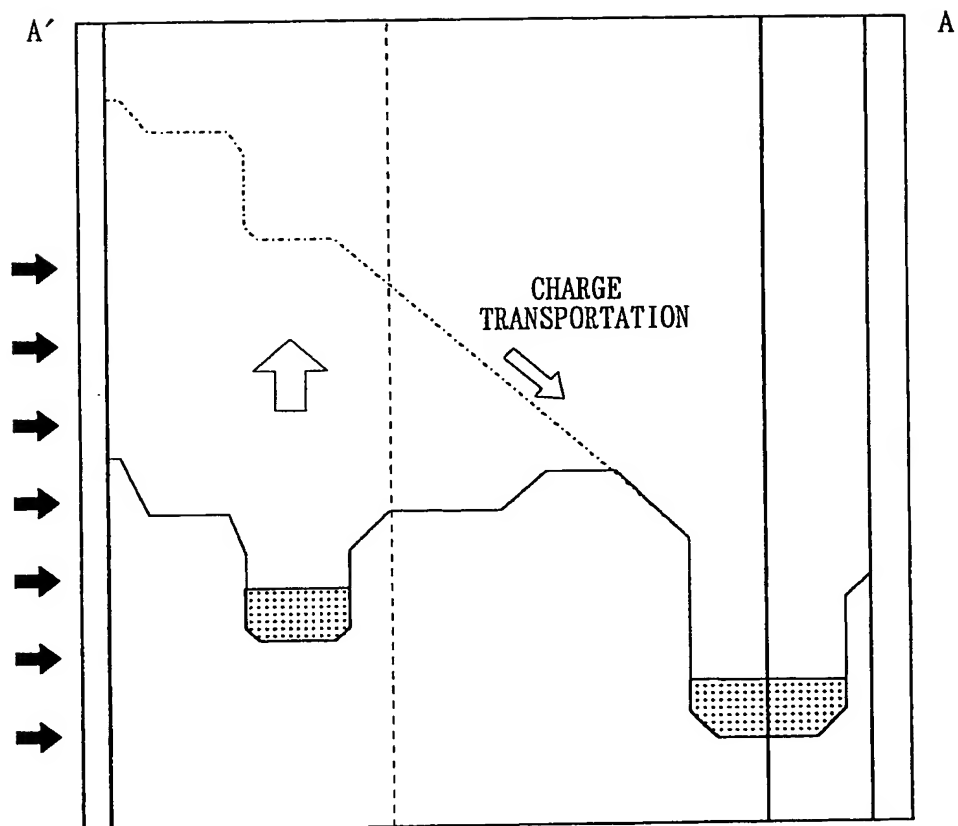


Fig. 23

551 IMAGE SENSOR

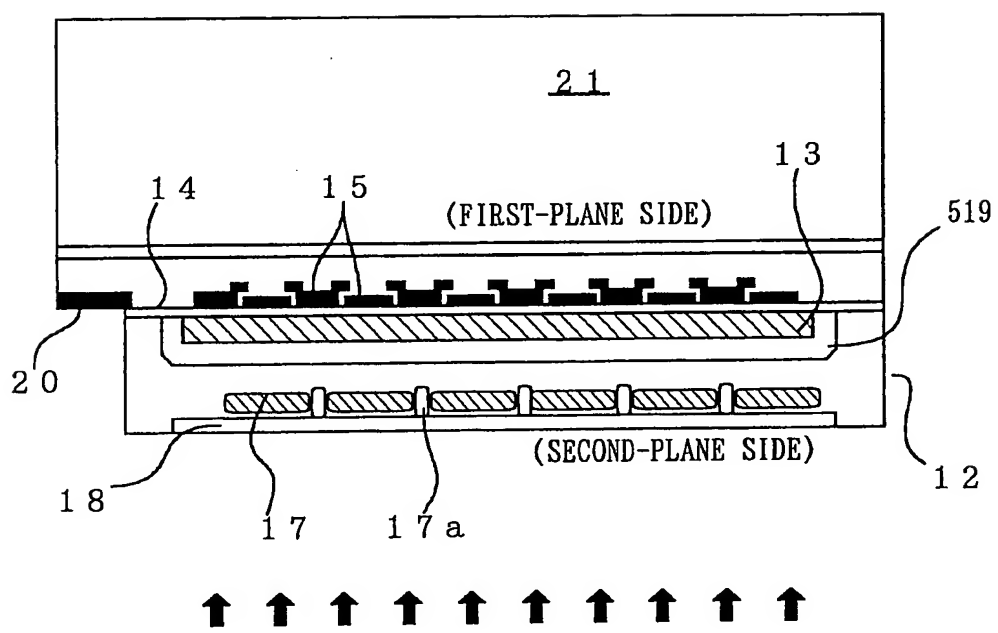


Fig. 24

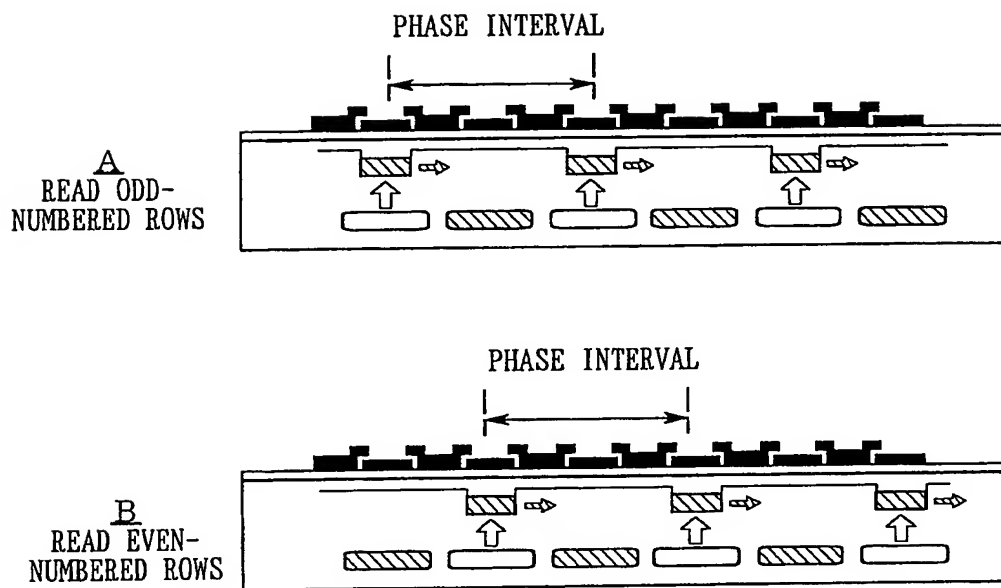


Fig. 25

552 IMAGE SENSOR

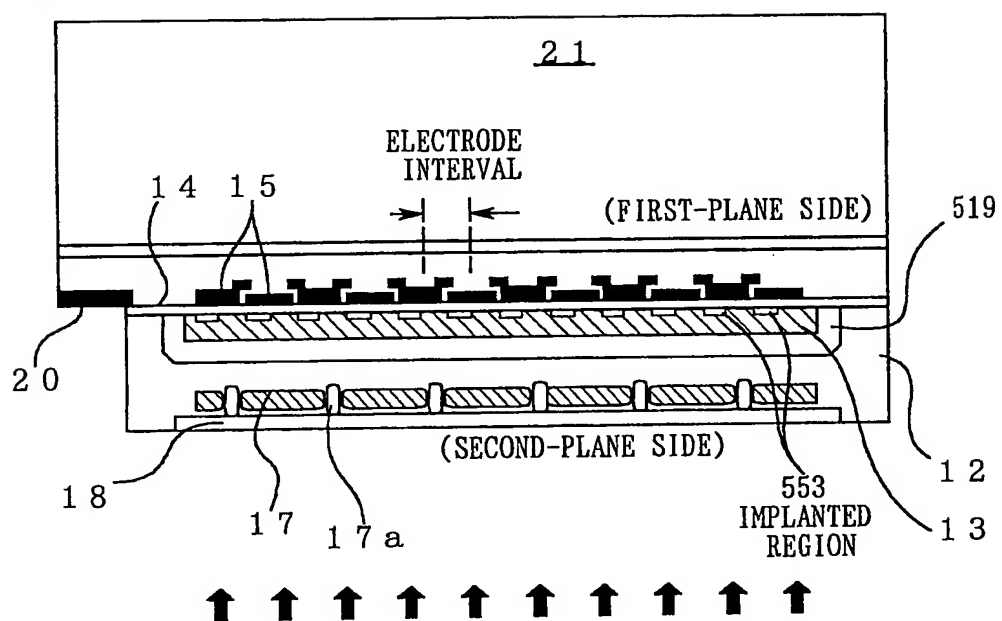


Fig. 26

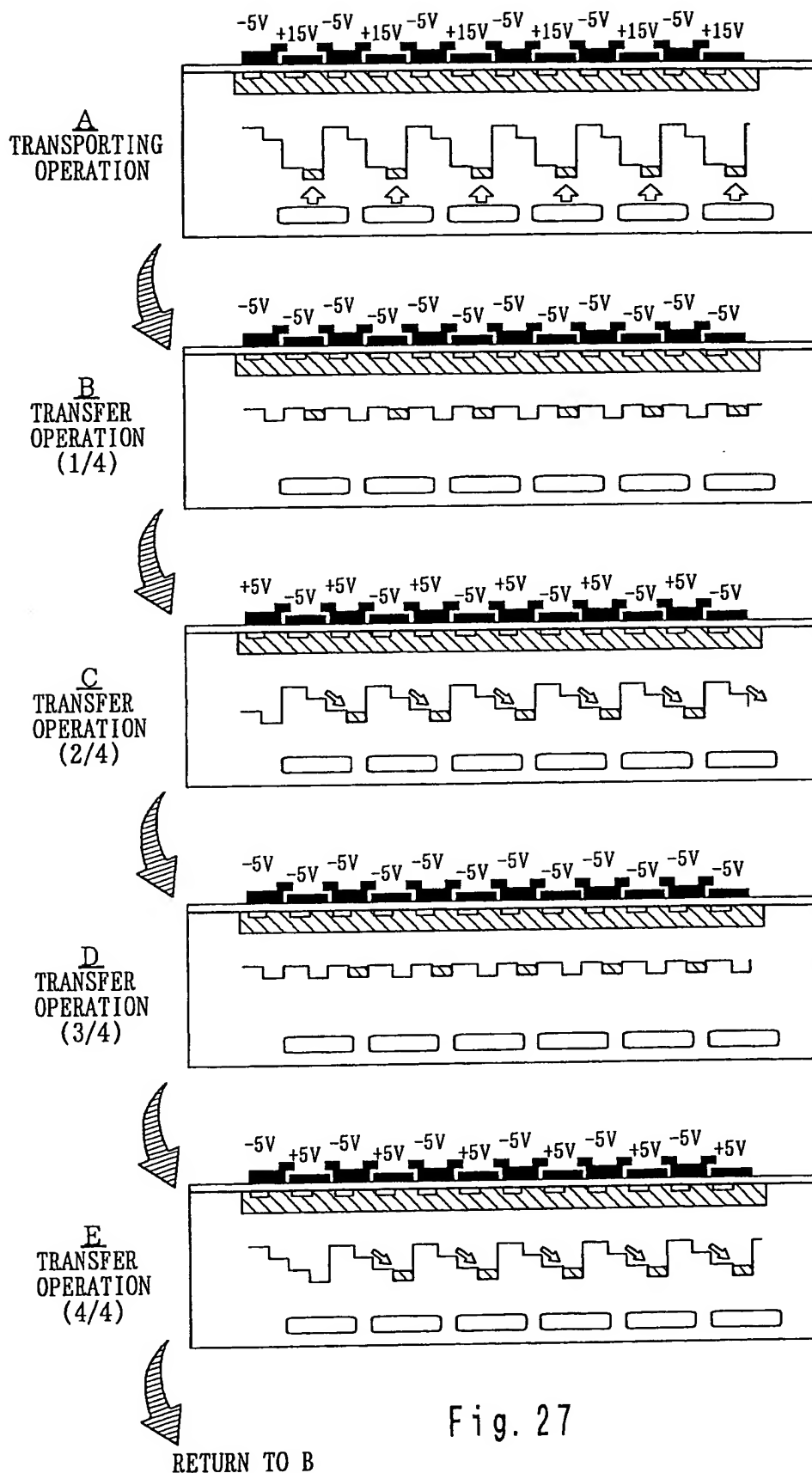


Fig. 27

6 0 EXPOSURE APPARATUS

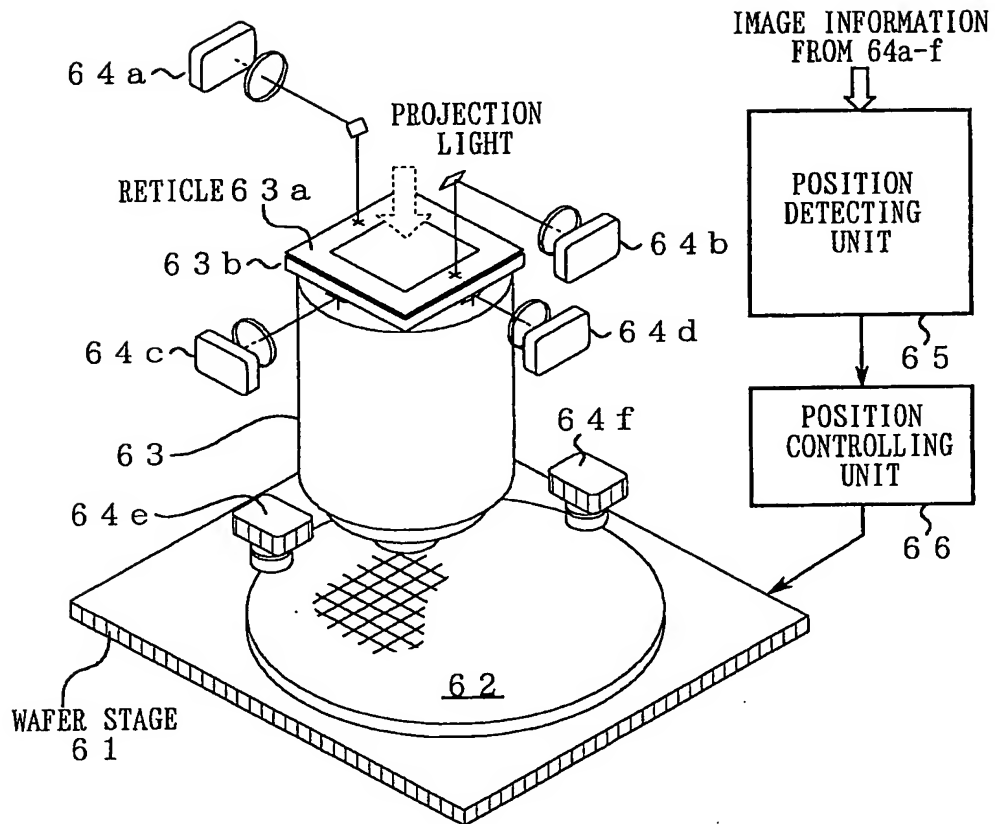


Fig. 28

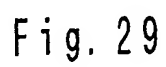


Fig. 29

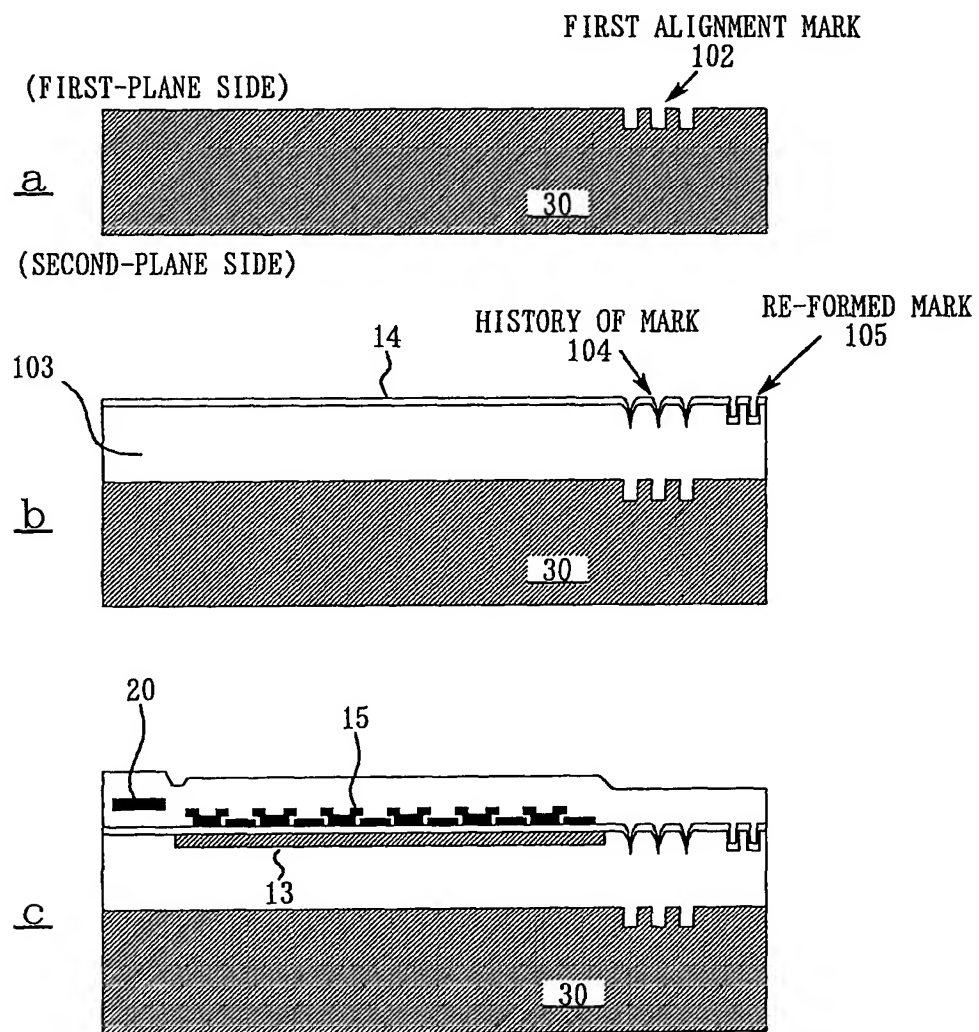


Fig. 30

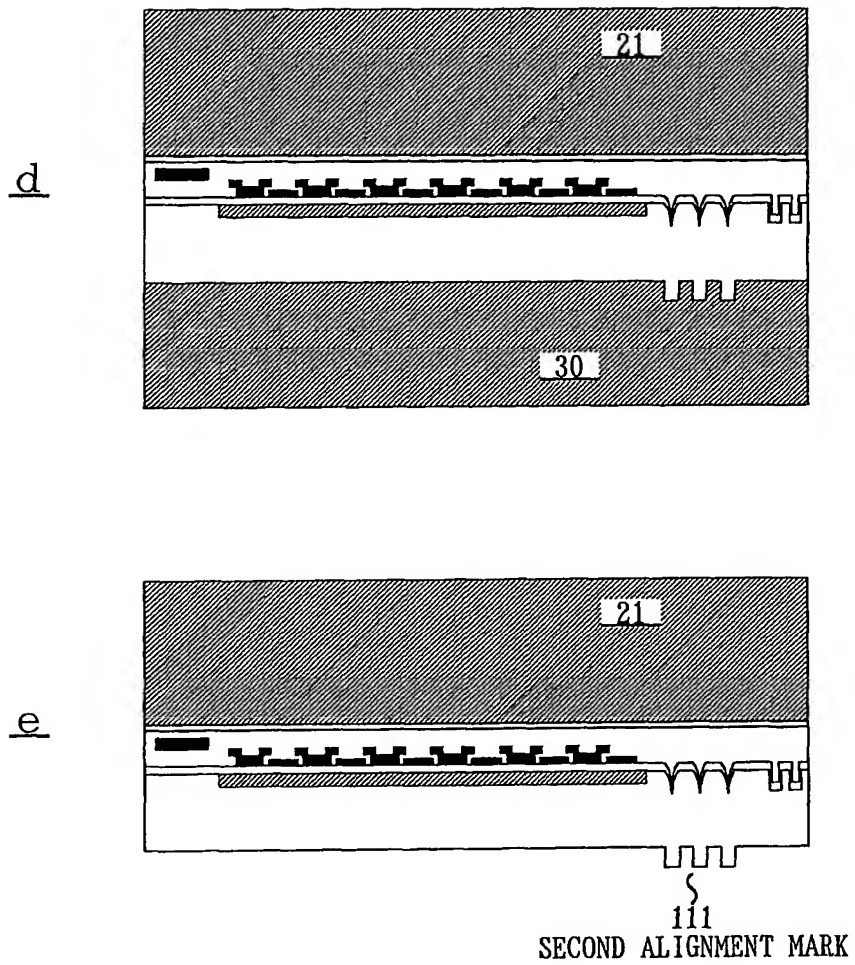


Fig. 31

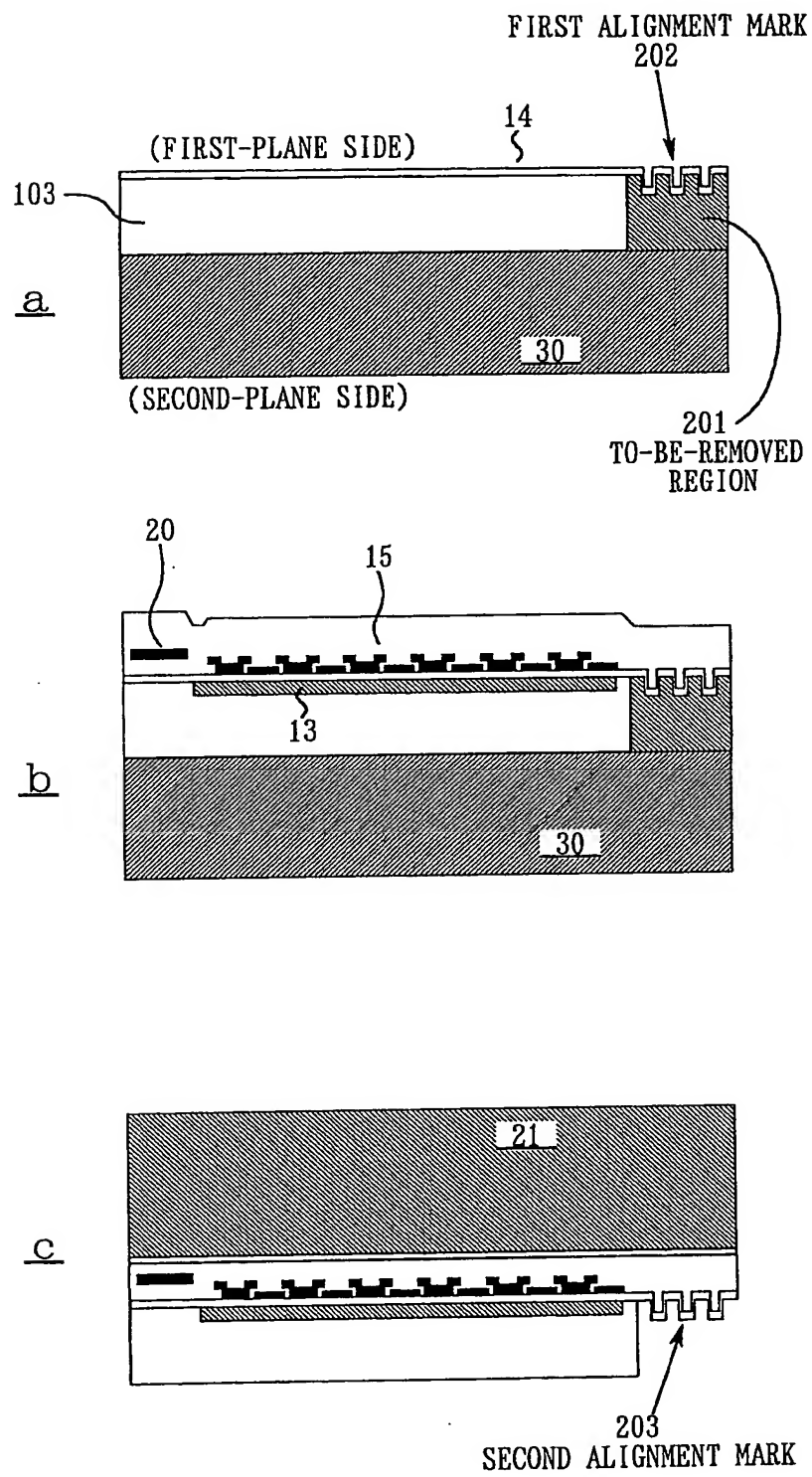


Fig. 32

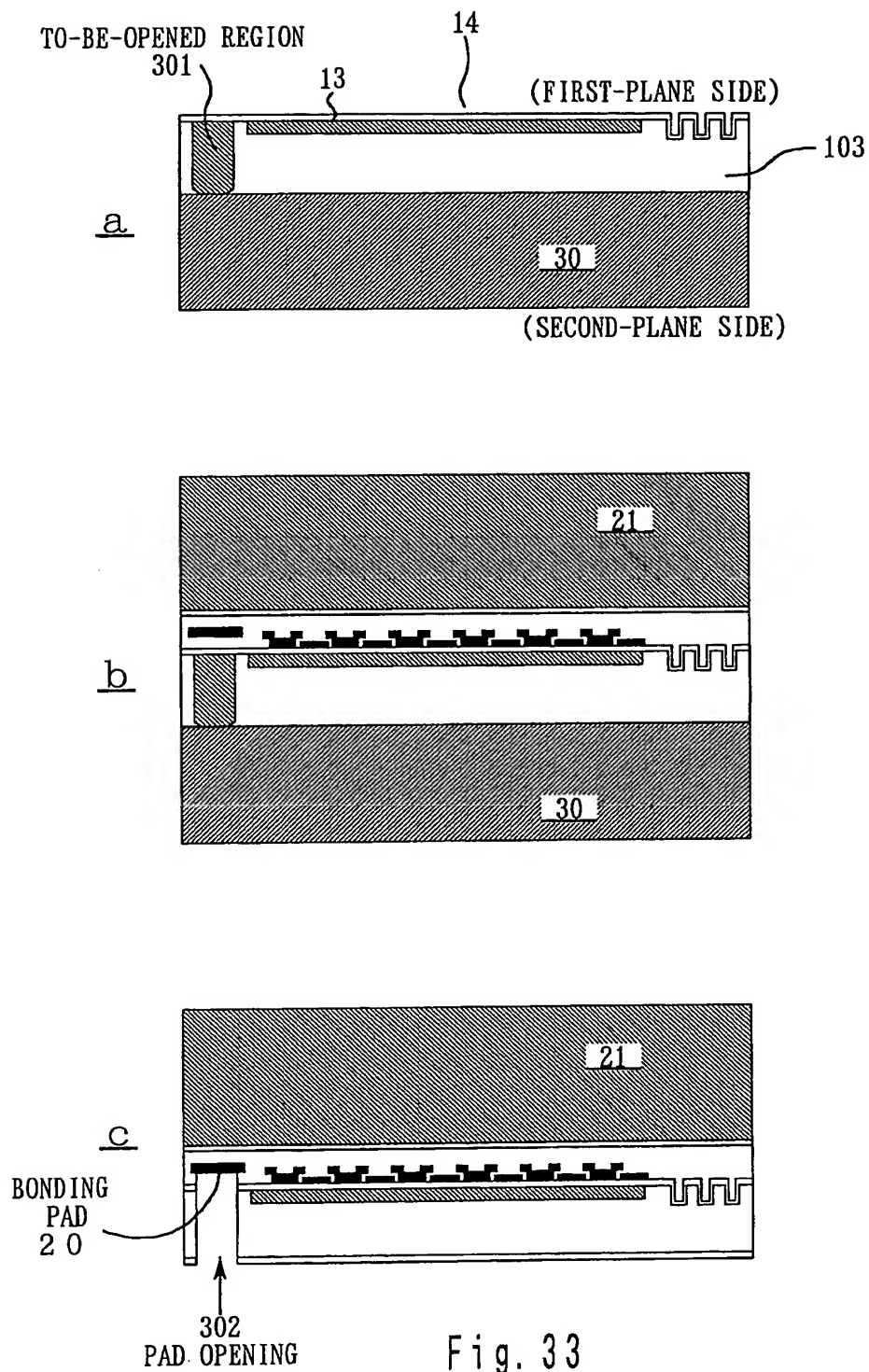


Fig. 33

8.1 IMAGE SENSOR

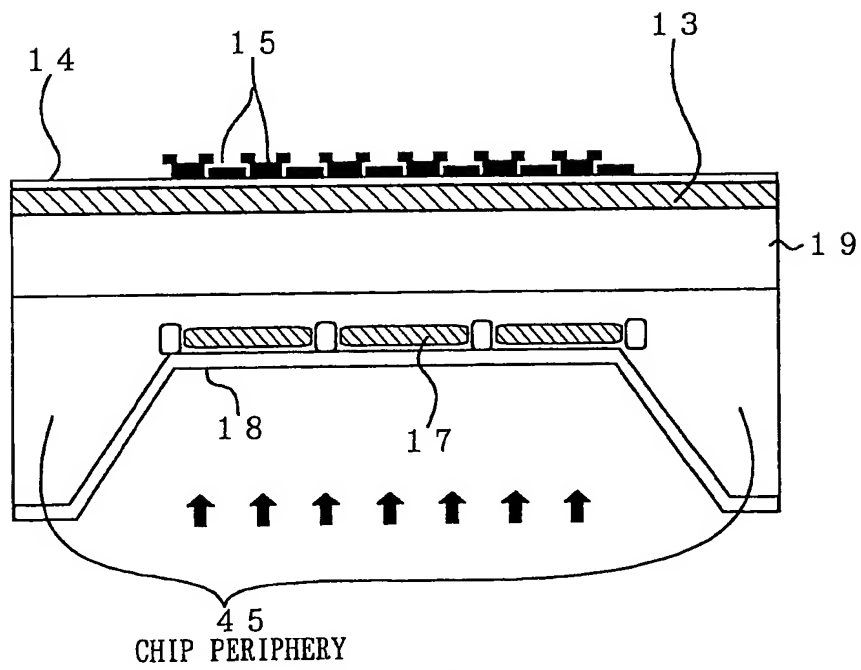


Fig. 34

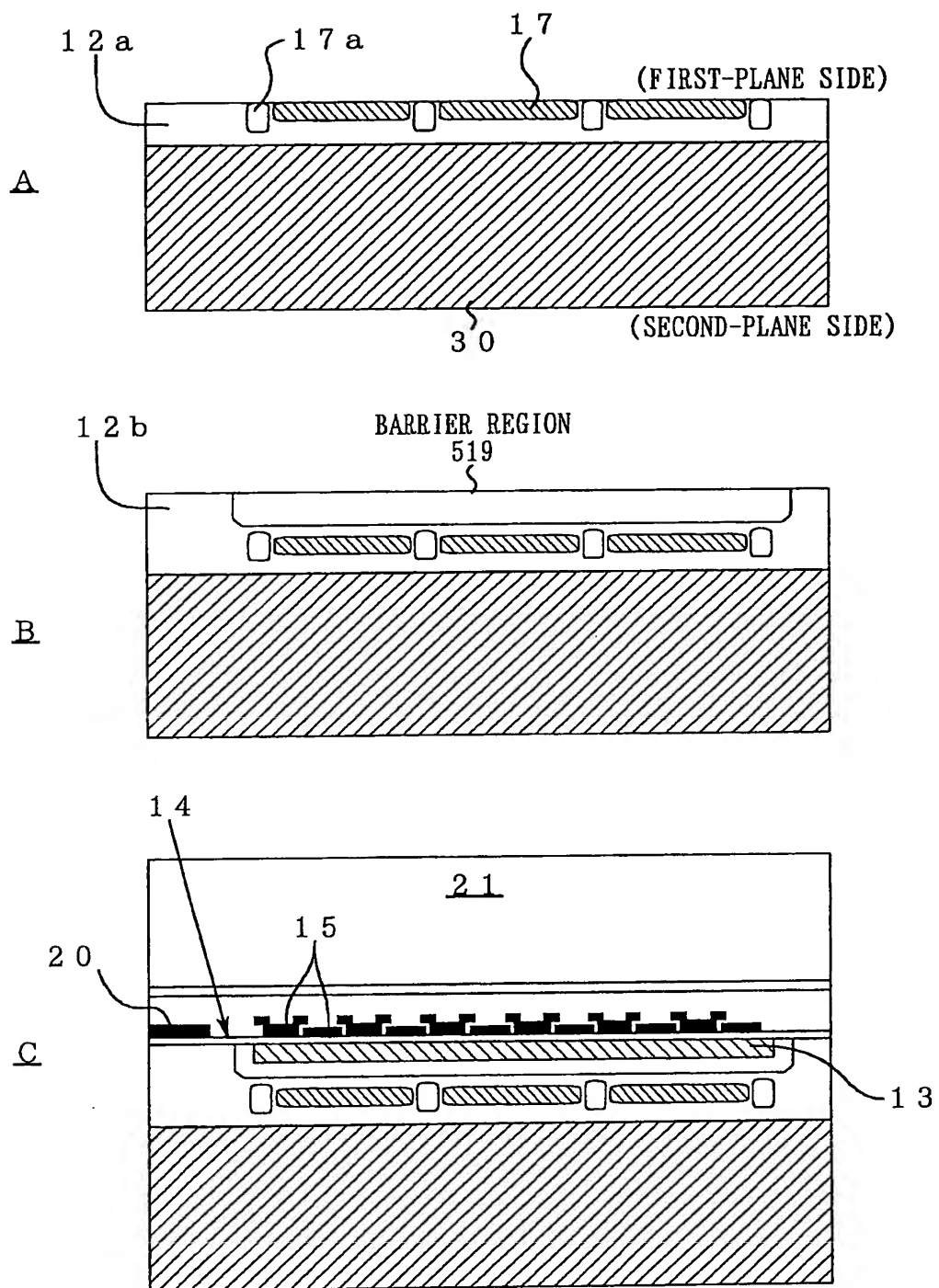


Fig. 35

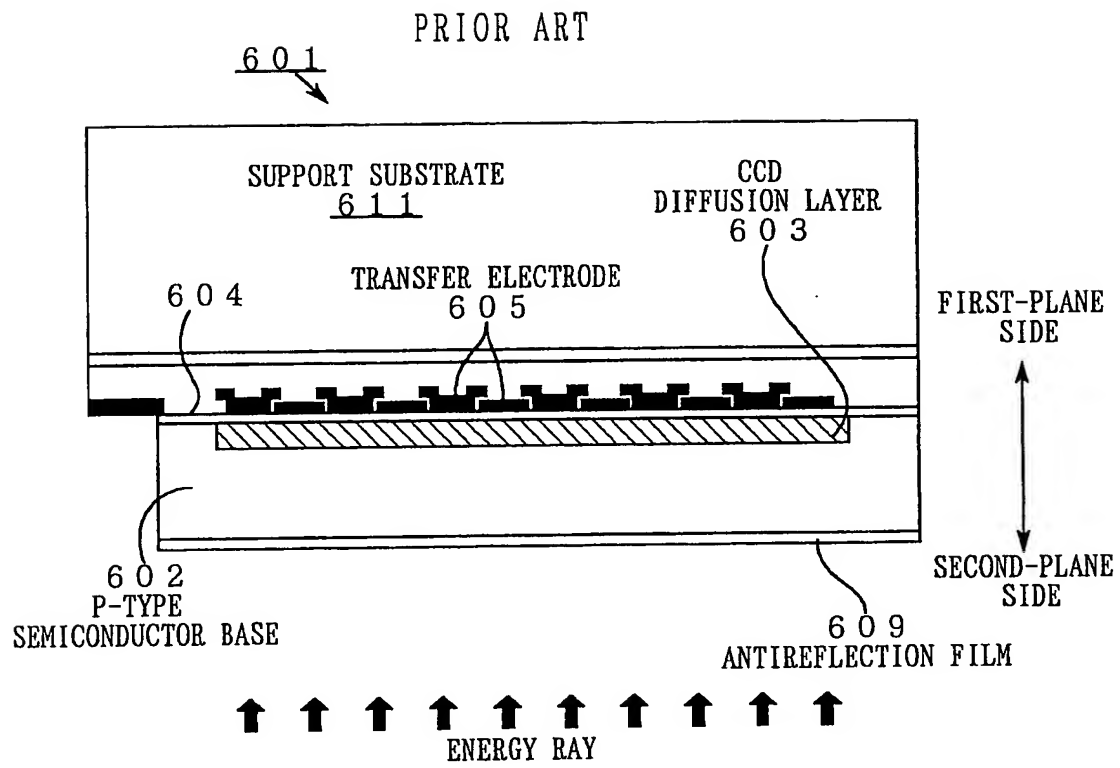


Fig. 36

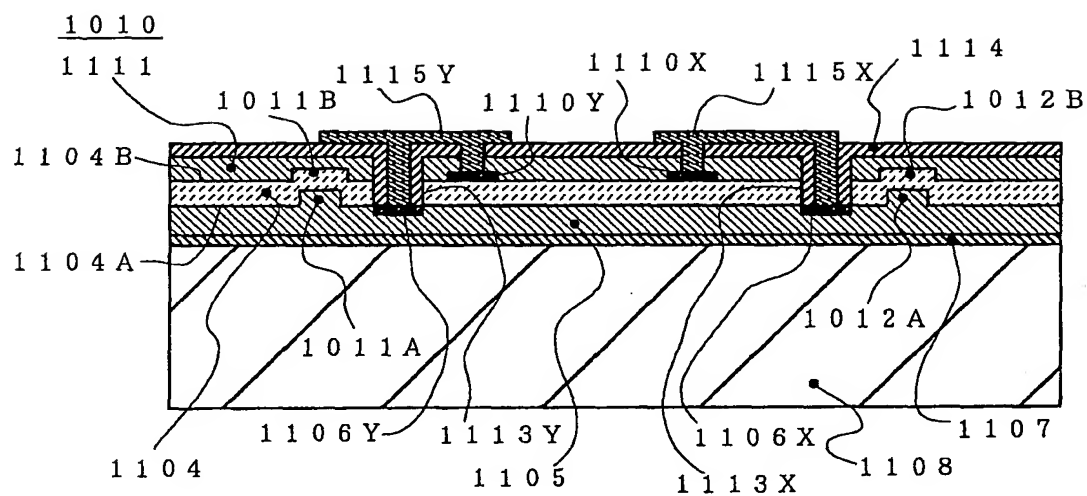


Fig. 37

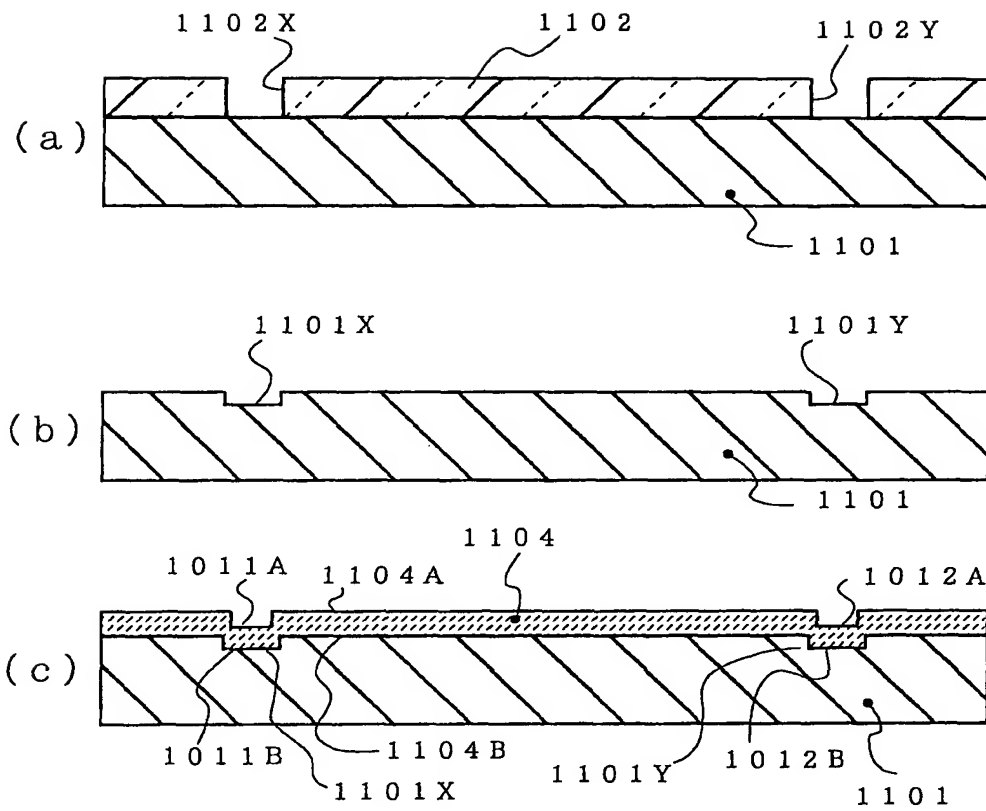


Fig. 38

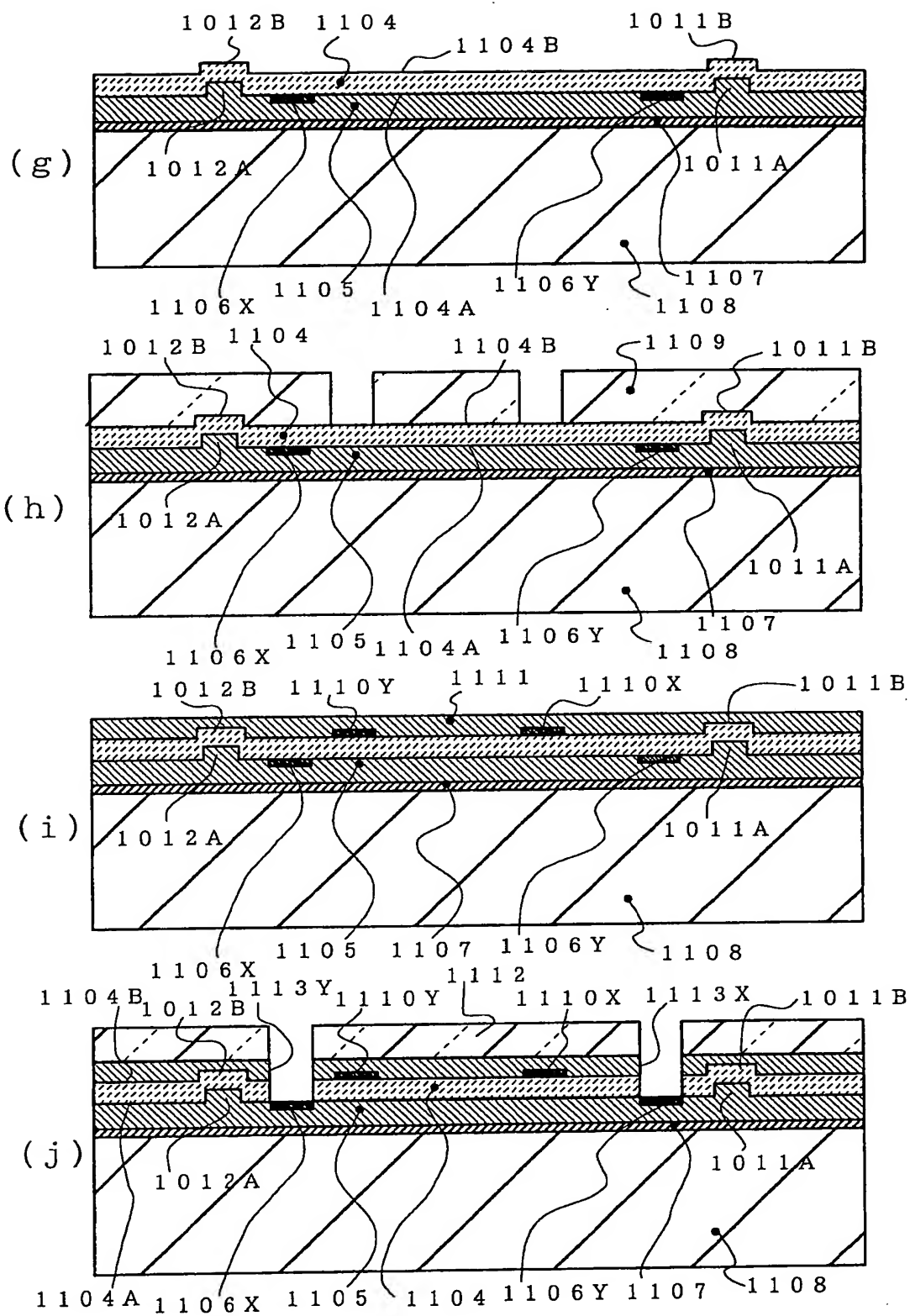


Fig. 40

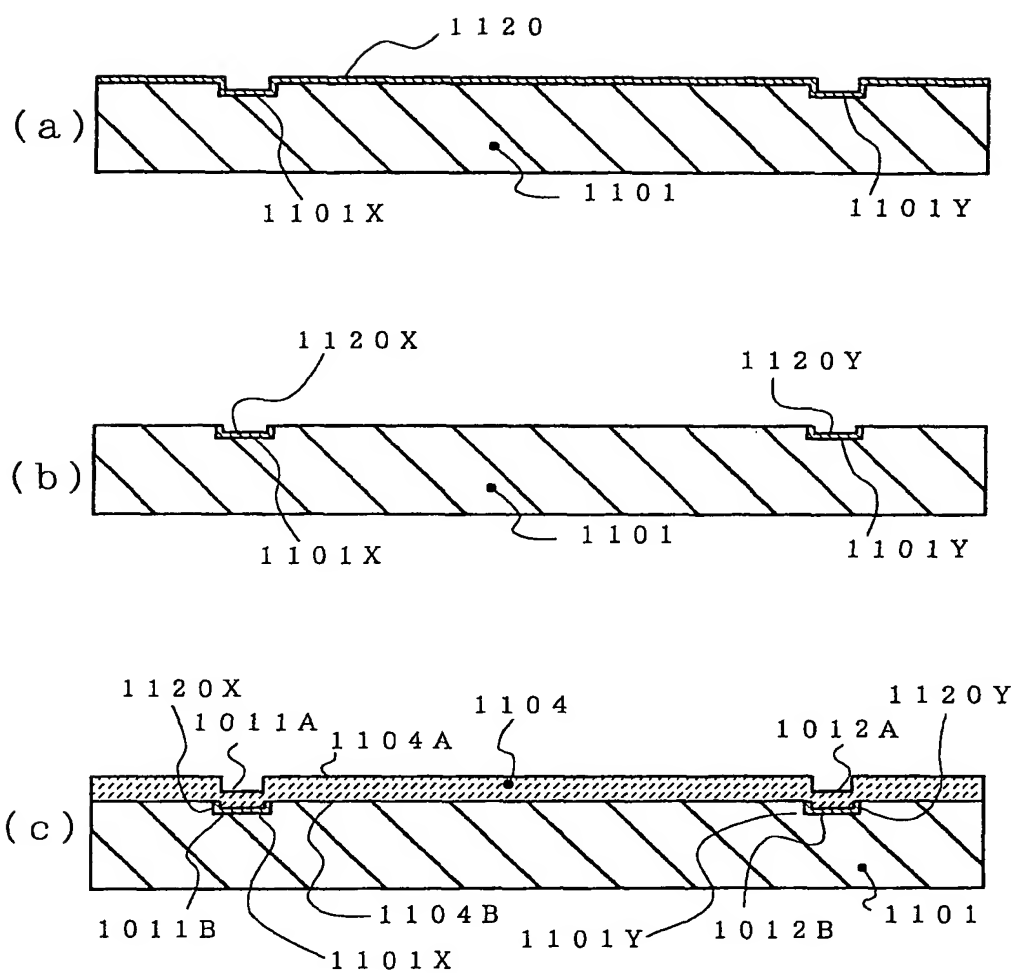


Fig. 41

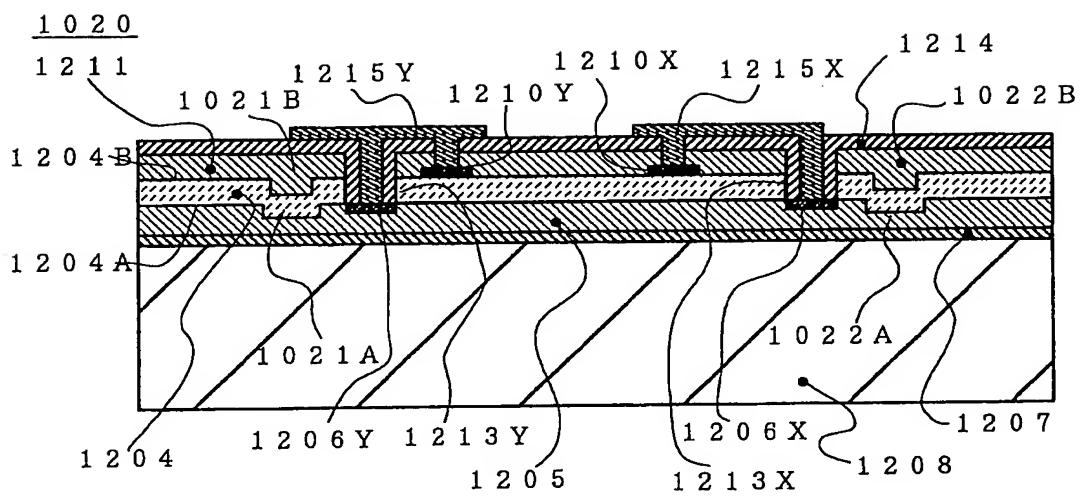


Fig. 42

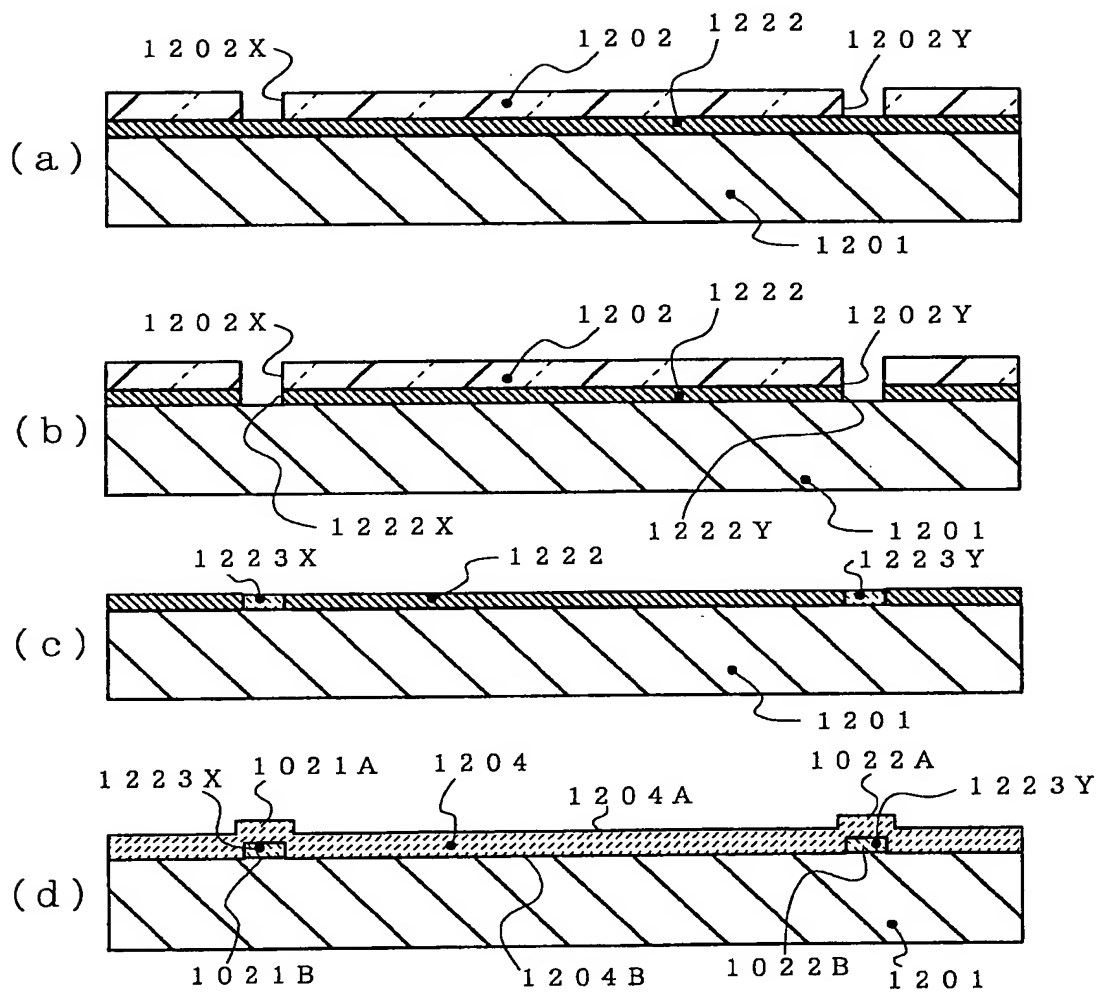


Fig. 43

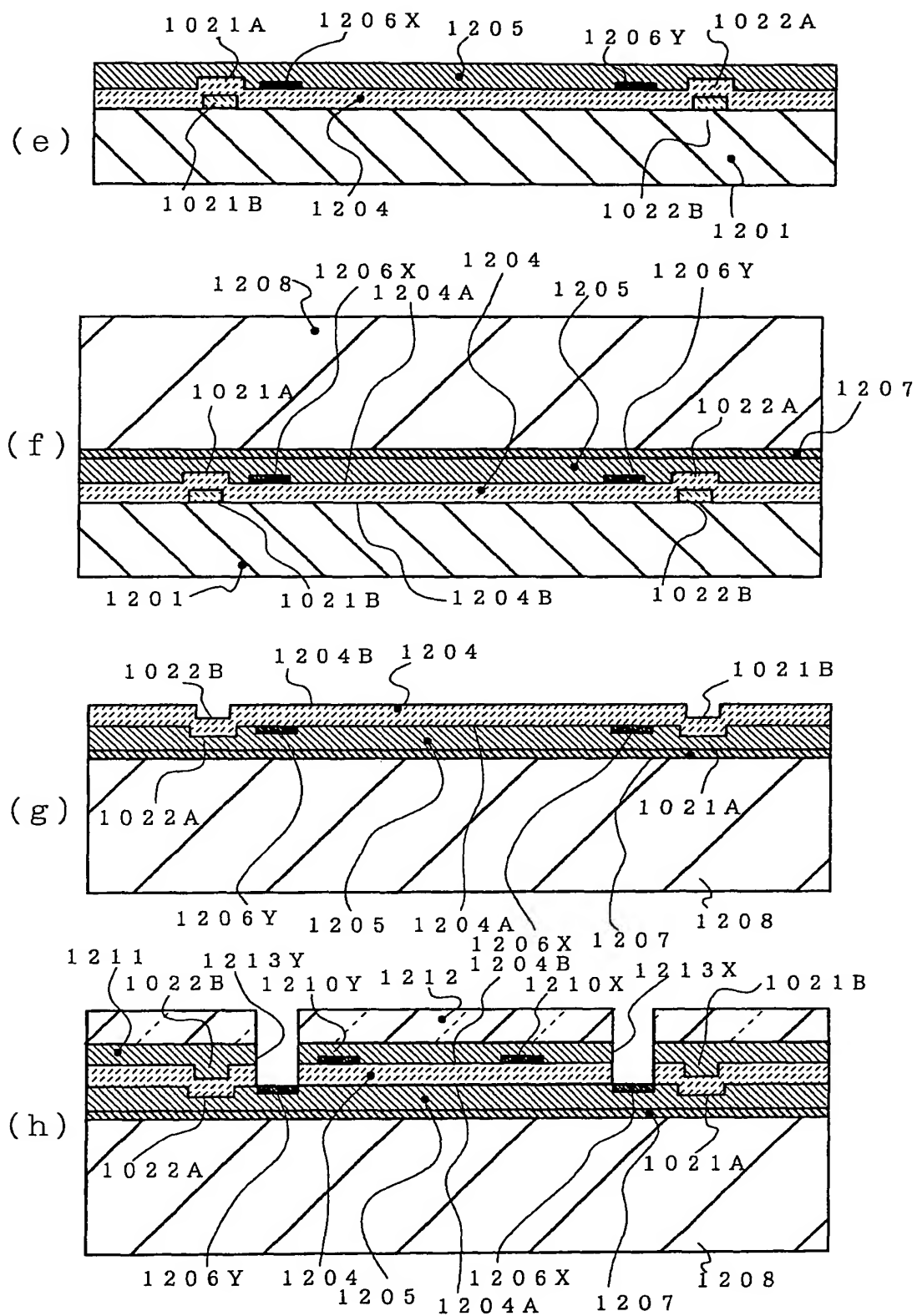


Fig. 44

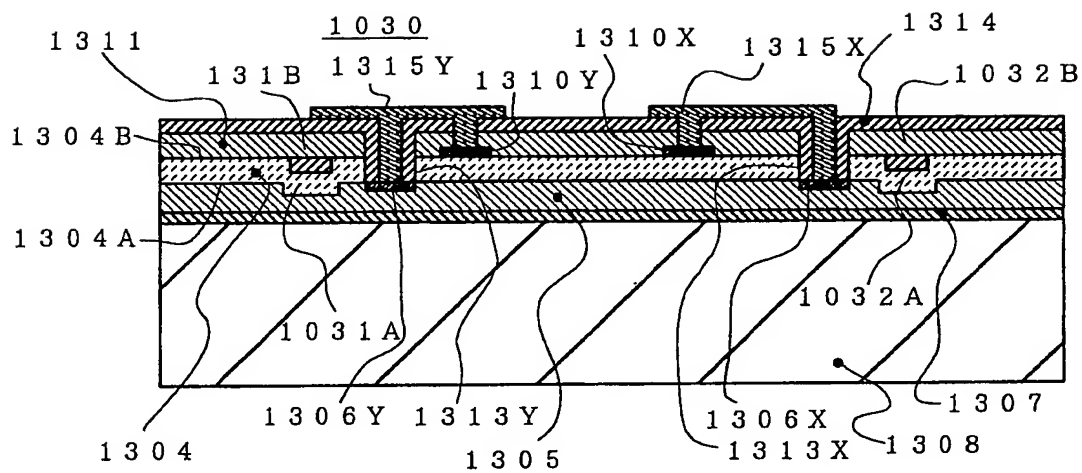


Fig. 45

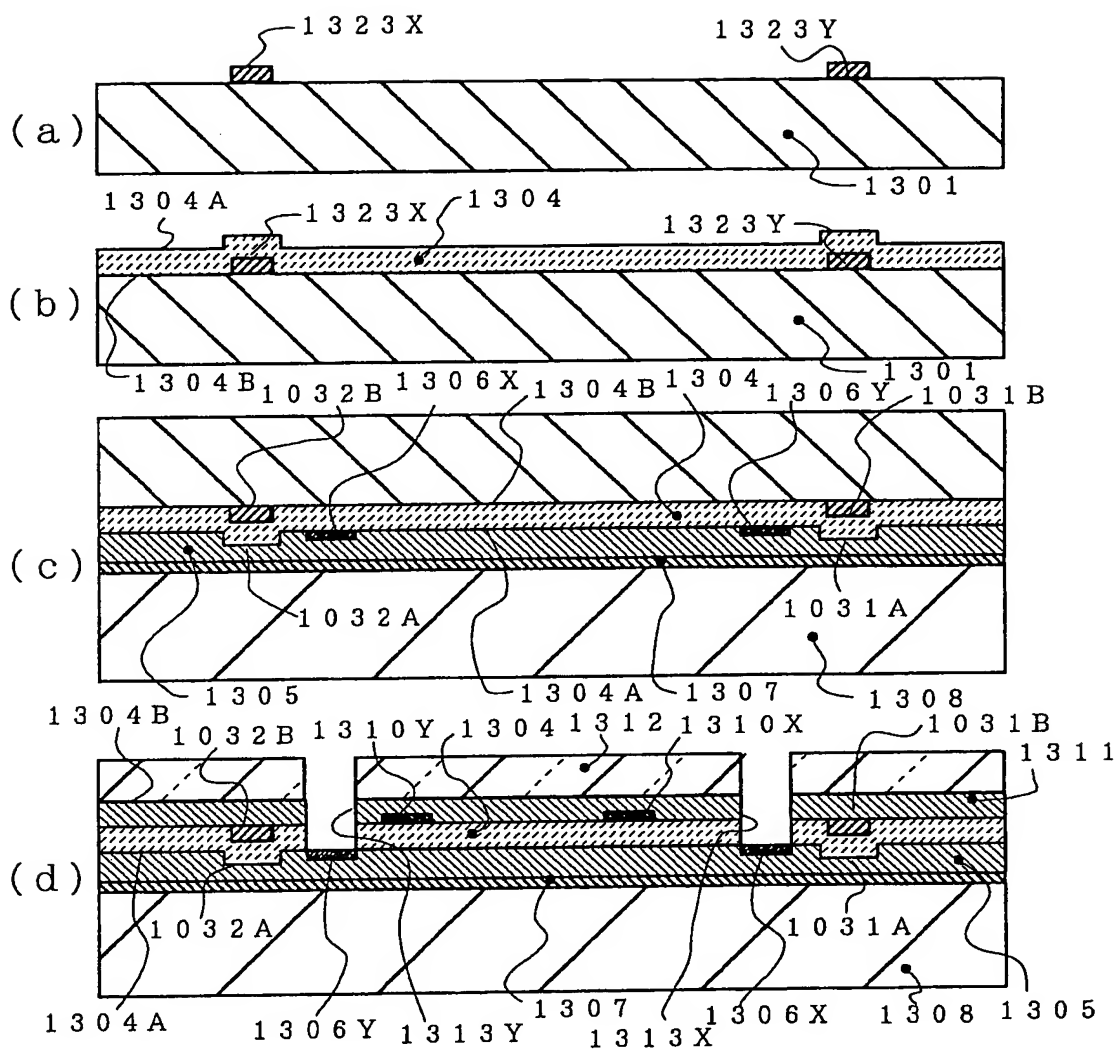


Fig. 46

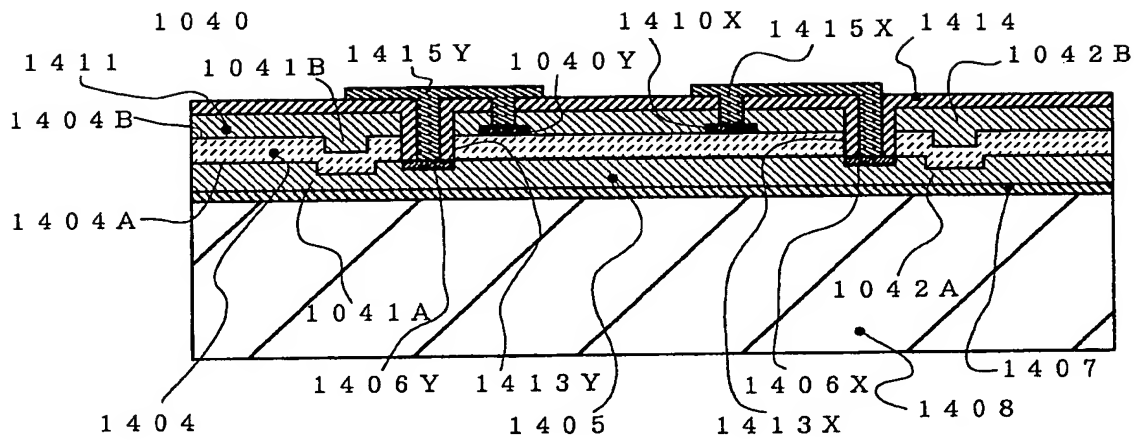


Fig. 47

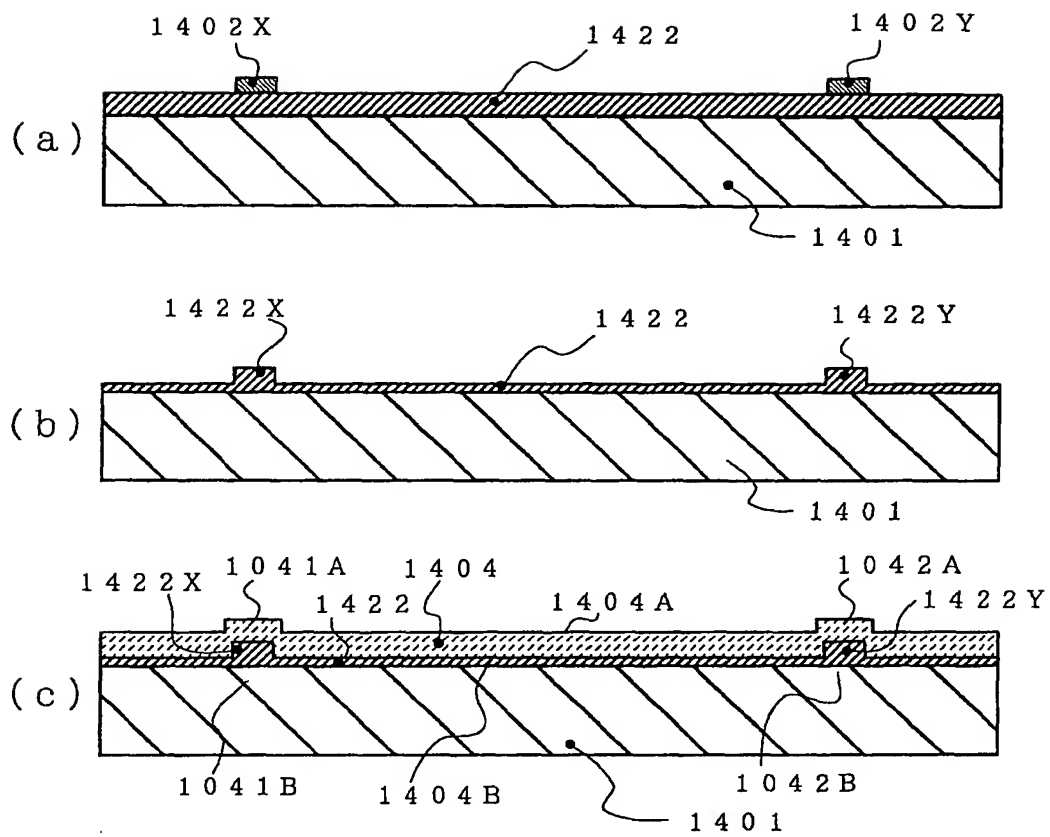


Fig. 48

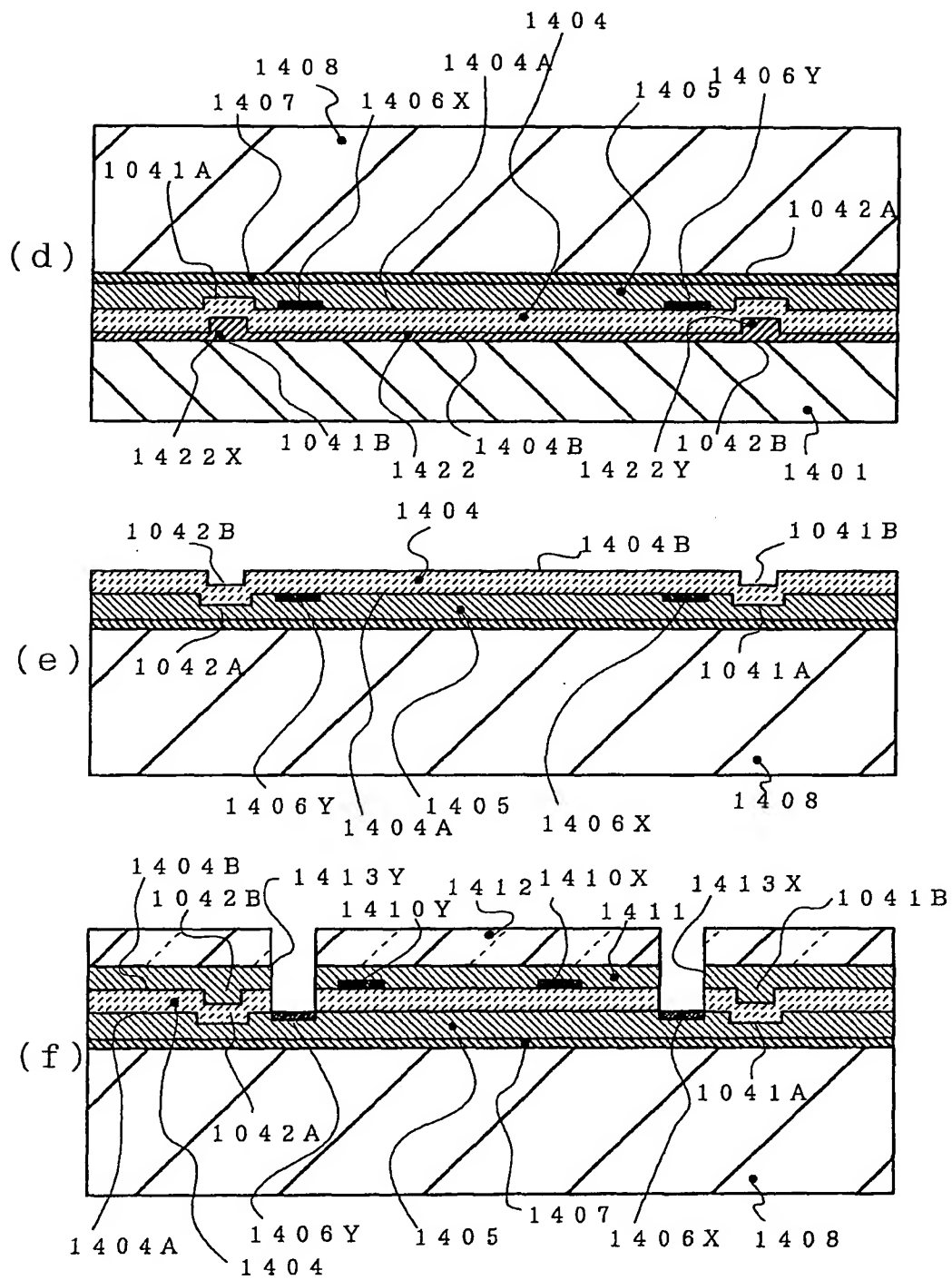


Fig. 49